

August 2006

FSQ510, FSQ510H — Green Mode Fairchild Power Switch (FPS[™]) for Quasi-Resonant Converter – Low EMI and High Efficiency

Features

- Uses a DMOS Integrated Power Switch
- Optimized for Quasi-Resonant Converter (QRC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High Efficiency through Minimum Voltage Switching
- Extended Quasi-Resonant Switching for Wide Load Ranges
- Small Frequency Variation for Wide Load Ranges
- Advanced Burst-Mode Operation for Low Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis
- Under-Voltage Lockout (UVLO) with Hysteresis
- Internal Start-up Circuit
- Internal High-Voltage SenseFET (700V)
- Built-in Soft Start (5ms)

Applications

- Cell Phone Chargers
- Auxiliary Power Supplies for PC and White Goods

Description

A Quasi-Resonant Converter (QRC) generally shows lower EMI and higher power conversion efficiency than a conventional hard-switched converter with a fixed switching frequency. The FSQ510(H) is an integrated controller Pulse-Width Modulation (PWM) SenseFET specifically designed for quasi-resonant offline Switch Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading Edge Blanking (LEB), optimized gate driver, internal soft start, temperaturecompensated precise current sources for loop compensation, and self-protection circuitry. Compared with discrete MOSFET and PWM controller solution, the FSQ510(H) can reduce total cost, component count, size and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform that is well suited for cost-effective designs of quasi-resonant switching flyback converters.

Ordering Information

One		Operating	Operating		Maximum Output Power (1)							
Part	Package	Pb-	Temperature		Temperature			230VAC ± 15% ⁽²⁾		85-265VAC		Replaces
Number	raonago	Free	Range	Limit	(MAX)	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Devices		
FSQ510	7-DIP	Yes	-25℃ to +85℃	320mA	32Ω	5W	7W	4W	5W	FSD210B		
FSQ510H	8-DIPH	Yes	-25℃ to +85℃	320mA	32Ω	5W	7W	4W	5W	FSD210HD		

Notes:

- 1. The junction temperature can limit the maximum output power.
- 230VAC or 100/115VAC with doubler.
- 3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
- 4. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Application Circuit

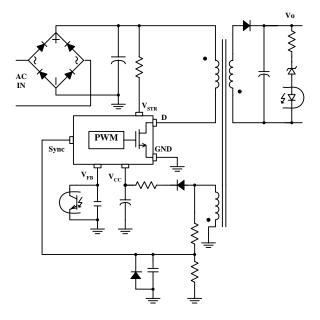


Figure 1. Typical Application Circuit

Internal Block Diagram

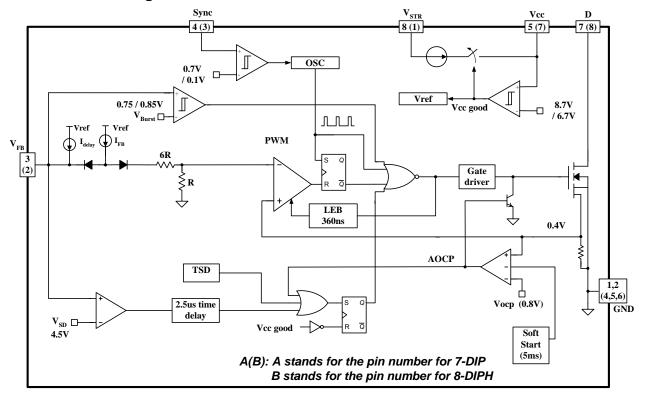


Figure 2. Internal Block Diagram

Pin Assignments

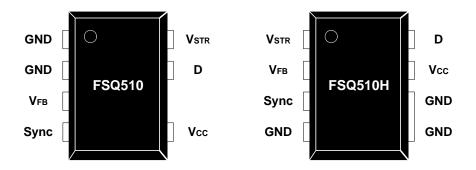


Figure 3. Package diagrams for FSQ510 and FSQ510H

Pin Definitions

Pin #	Name	Description
1,2 ⁽⁵⁾ (4,5,6) ⁽⁶⁾	GND	This pin is the control ground and the SenseFET source.
3 (2)	V _{FB}	This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 4.5V, the overload protection triggers, which shuts down the FPS.
4 (3)	Sync	This pin is internally connected to the sync-detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 0.7V/0.1V.
5 (7)	V _{CC}	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.
7 (8)	D	High-voltage power SenseFET drain connection.
8 (1)	V _{STR}	This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 8.7V, the internal current source is disabled.

Notes:

- 5. Pin numbers for 7-DIP.
- 6. Pin numbers for 8-DIPH are in parenthesis.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V _{STR}	V _{STR} Pin Voltage	700		V
V _{DS}	Drain Pin Voltage	700		V
V _{CC}	Supply Voltage		20	V
V_{FB}	Feedback Voltage Range	-0.3	6.5	V
V _{Sync}	Sync Pin Voltage	-0.3	6.5	V
P _D	Total Power Dissipation			W
T _J	Operating Junction Temperature		+150	°C
T _A	Operating Ambient Temperature	-25	+85	°C
T _{STG}	Storage Temperature	-55	+150	°C

Electrical Characteristics

 $T_J = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
SenseFET S	Section					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{CC} = 0V, I_D = 100 \mu A$	700			V
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} = 700V			100	μΑ
Б	Drain-Source On-State Resistance	$T_J = 25^{\circ}C, I_D = 180mA$		28	32	
$R_{DS(ON)}$	Dialii-Source Oil-State Resistance	$T_J = 100^{\circ}C, I_D = 180mA$		42	48	
C _{ISS}	Input Capacitance ⁽⁷⁾	V _{GS} = 11V		96		pF
Coss	Output Capacitance ⁽⁷⁾	V _{DS} = 40V		28		pF
t _r	Rise Time ⁽⁷⁾	$V_{DS} = 350V, I_{D} = 25mA$		100		ns
t_f	Fall Time ⁽⁷⁾	$V_{DS} = 350V, I_{D} = 25mA$		50		ns
Control Sec	ction					
f_S	Initial Switching Frequency	$V_{CC} = 11V, V_{FB} = 0.5V$	87.7	93.5	100	kHz
Δf_{S}	Switching Frequency Variation ⁽⁷⁾	- 25°C < T _J < 125°C		±5	±8	%
I_{FB}	Feedback Source Current	$V_{CC} = 11V$, $V_{FB} = 0V$	200	225	250	μΑ
t_{B}	Switching Blanking Time	V_{CC} = 11V, V_{FB} = 1V, V_{sync} oscillation	7.2	7.7	8.2	μS
t _W	Quasi-Resonant-Detection-Window Time	$V_{CC} = 11V$, $V_{FB} = 1V$, V_{sync} oscillation	2.8	3.0	3.2	μS
D _{MAX}	Maximum Duty Ratio	$V_{CC} = 11V$, $V_{FB} = 3V$	54	60	66	%
D _{MIN}	Minimum Duty Ratio	$V_{CC} = 11V, V_{FB} = 0V$			0	%
V _{START}	,	V _{FB} = 0V, V _{CC} sweep	8.0	8.7	9.4	V
V _{STOP}	UVLO Threshold Voltage	After Turn-on, V _{FB} = 0V	6.0	6.7	7.4	V
t _{S/S}	Internal Soft-Start Time	V _{STR} = 40V, V _{CC} sweep	3	5	7	ms
Burst-Mode	Section					
V_{BURH}			0.75	0.85	0.95	V
V_{BURL}	Burst-Mode Voltage	V_{CC} = 11V, V_{FB} sweep	0.65	0.75	0.85	V
Hys.				100		mV
Protection	Section					
I _{LIM}	Peak Current Limit	di/dt = 150mA/μs	280	320	360	mA
V_{SD}	Shutdown Feedback Voltage	$V_{DS} = 40V$, $V_{CC} = 11V$, V_{FB} sweep	4.0	4.5	5.0	V
I _{DELAY}	Shutdown Delay Current	V _{CC} = 11V, V _{FB} = 5V	4	5	6	μΑ
t _{LEB}	Leading Edge Blanking Time ⁽⁷⁾		-	360	-	ns
V _{OCP}	Over-Current Latch Voltage ⁽⁷⁾		-	0.8	-	V
T_{SD}	Thermal Shutdown Temperature ⁽⁷⁾		130	140	150	°C
Hys.	Thermal Shuldown Temperalure			60		°C
Sync Section						
V_{SH}	Sync Threshold Voltage	V _{CC} = 11V, V _{FB} = 1V	0.55	0.7	0.85	V
V _{SL}	Sync Theshold Voltage	V _{CC} = 11V, V _{FB} = 1V	0.05	0.1	0.15	V
t _{Sync}	Sync Delay Time		180	200	220	ns
Total Devic	e Section					
I _{OP}	Operating Supply Current (Control Part Only)	$V_{CC} = 11V, V_{FB} = 3V$		500	900	μА
I _{CH}	Start-up Charging Current	$V_{CC} = V_{FB} = 0V$, $V_{STR} = 40V$		1	1.2	mA
V_{STR}	Supply Voltage	$V_{CC} = V_{FB} = 0V,$ V_{STR} sweep	50		700	V

Notes:

7. These parameters, although guaranteed, are not 100% tested in production

Comparison between FSD210B and FSQ510

Function	FSD210B	FSQ510	Advantages of FSQ510
Control Mode	control Mode Voltage Mode Current Mode		■ Fast response
			Easy to design control loop
Operation Method	Constant Frequency	Quasi-Resonant	■ Turn-on at minimum drain voltage
Operation Method	PWM	Operation	■ High efficiency
EMI Reduction	Frequency Modulation	Valley Switching	■ Frequency variation depending on the ripple of DC link voltage
Method		valley Switching	J 11
			High efficiency and low EMI
Soft Start	3ms (Built-in)	5ms (Built-in)	■ Longer soft-start time
Protection	TSD	TSD with hysteresis AOCP	■ Enhanced Thermal Shutdown protection ■ Abnormal Over-Current protection

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 4. When V_{CC} reaches 8.7V, the FPS begins switching and the internal high-voltage current source is disabled. The FPS continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 6.7V.

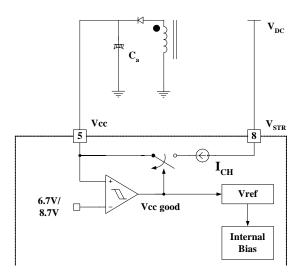


Figure 4. Startup Block

- 2. Feedback Control: FPS employs current mode control, as shown in Figure 5. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the $R_{\rm sense}$ resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This event typically occurs when the input voltage is increased or the output load is decreased.
 - 2.1 Pulse-by-Pulse Current Limit: Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (Vfb*), as shown in Figure 5. Assuming that the 225µA current source flows only through the internal resistor (6R + R = 11 k Ω), the cathode voltage of diode D2 is about 2.5V. Since D1 is blocked when the feedback voltage (Vfb) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the SenseFET is limited.

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

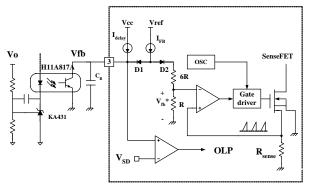


Figure 5. Pulse-Width Modulation (PWM) Circuit

3. Synchronization: The FSQ-series employs a quasi-resonant switching technique to minimize the switching noise and loss. The basic waveforms of the quasi-resonant converter are shown in Figure 6. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 6. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 6.

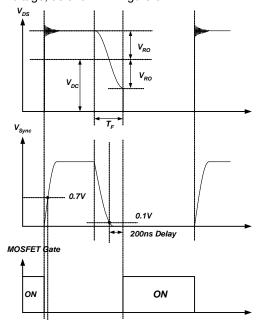


Figure 6. Quasi-Resonant Switching Waveforms

4. Protection Circuits: The FSQ-series has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart mode. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under-Voltage Lockout (UVLO) stop voltage of 6.7V, the protection is reset and the start-up circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 8.7V, the FSQ-series resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

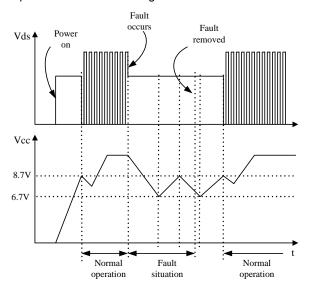


Figure 7. Auto Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the

feedback voltage (Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 5µA current source starts to charge $C_{\rm B}$ slowly up to $V_{\rm CC.}$ In this condition, Vfb continues increasing until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 8. The delay time for shutdown is the time required to charge $C_{\rm B}$ from 2.5V to 4.5V with 5µA. A 20 \sim 50ms delay time is typical for most applications. This protection is implemented in auto restart mode.

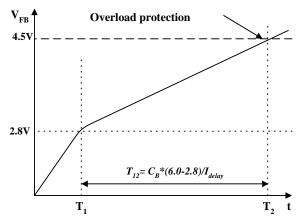


Figure 8. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FSQ-series has OLP (Overload Protection), it is not enough to protect the FSQ-series in this abnormal case, since severe current stress is imposed on the SenseFET until OLP triggers. The FSQ-series has an internal AOCP circuit, as shown in Figure 9. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

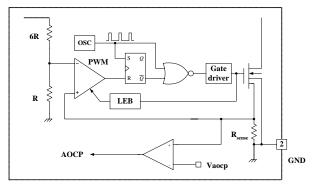


Figure 9. Abnormal Over-Current Protection

- **4.3 Thermal Shutdown (TSD)**: The SenseFET and the control IC in one package makes it easy for the control IC to detect the abnormal over temperature of the SenseFET. If the temperature exceeds approximately 140°C, the thermal shutdown triggers. The FPS stops its operation at that time. The FPS operates in auto-restart mode until the temperature decreases to around 80°C. Then the normal operation of the FPS resumes.
- **5. Soft Start**: The FPS has an internal soft-start circuit that increases PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts up. The typical soft-start time is 5ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This helps prevent transformer saturation and reduce stress on the secondary diode during startup.
- **6. Burst-Mode Operation**: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 10, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (850mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

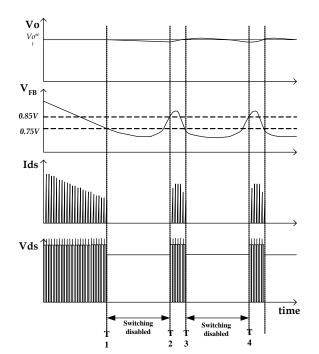


Figure 10. Burst-Mode Operation

7. Advanced Quasi-Resonant Operation: To minimize switching loss and Electromagnetic Interference (EMI). the MOSFET turns on when the drain voltage reaches its minimum value in QRC converters. Due to Discontinuous Conduction Mode (DCM) operation, the feedback voltage is not changed, despite the DC link voltage ripples, if the load condition is not changed. Since the slope of the drain current is changed depending on the DC link voltage, the turn-on duration of MOSFET is variable with the DC link voltage ripples. The switching period is changed continuously with the DC link voltage ripples. Not only the switching at the instant of the minimum drain voltage, but also the continuous change of the switching period, reduces EMI. So QRC converters can scatter the EMI spectrum inherently.

Typical products for QRC turn on the MOSFET when the first valley is detected. In this case, the range of the switching frequency is very wide as a result of the load variations. At a very light load, for example, the switching frequency can be as high as several hundred kHz. Some products for QRC, such as Fairchild's FSCQ-series, define the turn-on instant of SenseFET change at the first valley into at the second valley when the load condition decreases under its predetermined level. The range of switching frequency narrows somewhat. For details, consult an FSCQ-series datasheet at:

http://www.fairchildsemi.com/pf/FS/FSCQ1265RT.html

The range of the switching frequency can be limited tightly in FSQ-series. Because a kind of blanking time (t_B) is adopted, as shown in Figure 11, the switching frequency has minimum and maximum values.

Once the SenseFET is enabled, the next start is prohibited during the blanking time (t_B). After the blanking time, the controller finds the first valley within the duration of the quasi-resonant detection window time (t_W) (Case A, B, and C). If no valley is found in t_W , the internal SenseFET is forced to turn on at the end of t_W (Case D). Therefore, FSQ510 and FSQ510H have minimum switching frequency of 93.5kHz and maximum switching frequency of 130kHz, as shown in Figure 12.

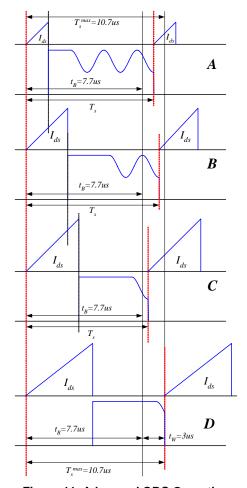


Figure 11. Advanced QRC Operation

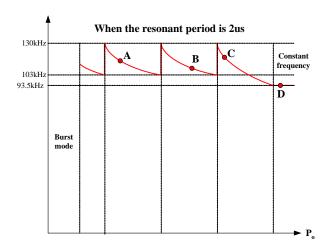


Figure 12. Switching Frequency Range of the Advanced QRC

Application Information

Application	Output Power	Input Voltage	Output Voltage (Max Current)
Cellular Phone Charger	3.3W	Universal Input (85-265Vac)	5.1V (650mA)

Features

- Low-cost, no Y-cap, cellular phone charger with CC/CV function
- Meets CISPR-22 Class-B requirement at full-load condition
- Meets CEC & Energy Star EPS program (arithmetic average of efficiencies at 25%, 50%, 75%, and 100% of full load measured at the end of 0.2 \(\text{\subset} / 1.5 \text{m load line, enclosed in plastic case, room temperature, still air)}
- Extremely low no-load standby power (<60mW at universal input)

Key Design Notes

- The constant voltage (CV) mode control is implemented with resistors R2, R4, R5, and R6; feedback capacitor C8; shunt regulator of U1; and opto-coupler U3.
- The constant current (CC) mode control is designed with resistors R2, R4, R10, R11, R13, and R14; NPN transistor Q1; and NTC THR1.
- The divided bias winding voltage is applied to the sync pin with resistor R12, R15, and R16. The capacitor C9 is added to delay the divided bias winding for switching at the minimum drain voltage. The diode D7 is used to avoid a significant negative voltage on the sync pin.

1. Schematic

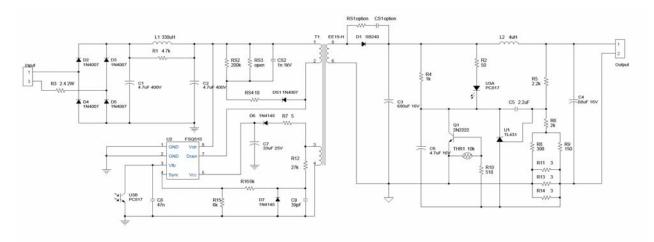


Figure 13. FSQ510 Schematic

2. Transformer Construction

Core: EE1616 (PM7/ Ae=20.5mm²)

■ Bobbin: Horizontal 8 pins, 4 pins at each side, 10mm width (bobbin wall-to-wall)

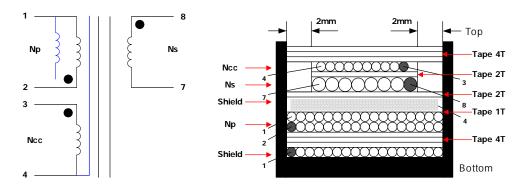


Figure 14. Transformer Construction Illustration

3. Winding Specifications

	Pin (S \rightarrow F)	Wire	Turns	Winding Method		
Shield	1 → X	0.16φ×1	48 Ts	Solenoid winding		
	Insulati	on: Polyester Tape t = 0).025mm, 4 La	ayers		
Np	2 → 1	0.16φ×1	92 Ts	Solenoid winding		
	Insulation: Polyester Tape t = 0.025mm, 1 Layer					
Shield	4 → X	Copper 8mm× 0.05t	0.9 Ts	Copper Plate		
	Insulati	on: Polyester Tape t = 0	0.025mm, 2 La	ayers		
Ns	8 → 6	0.55φ×1	5 Ts	Solenoid winding Barrier Tape 2mm		
	Insulation: Polyester Tape t = 0.025mm, 2 Layers					
Ncc	3 → 4	0.16φ×2	11 Ts	Center Solenoid winding Barrier Tape 2mm		
	Insulation: Polyester Tape t = 0.025mm, 4 Layers					

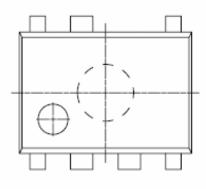
4. Electrical Characteristics

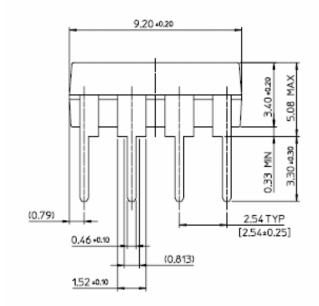
	Pin	Specification	Remark
Inductance	1-2	1.2mH ± 10%	100kHz, 1V
Leakage	1-2	60μH maximum	Short 2nd pins

5. BOM List

Number	Quantity	Description	Reference Number	Part Type
1	2	Electrolytic Cap.	C1, C2	4.7µF, 400V
2	1	Electrolytic Cap.	C3	680μF, 16V
3	1	Electrolytic Cap.	C4	68μF, 16V
4	1	Ceramic Cap.	C5	2.2µF
5	1	Electrolytic Cap.	C6	4.7µF, 50V
6	1	Electrolytic Cap.	C7	47μF, 50V
7	1	Ceramic Cap.	C8	47nF
8	1	Ceramic Cap.	C9	39pF
9	1	Film Cap.	CS2	1nF, 1kV
10	1	Schottky Diode	D1	SB240
11	5	Diode	D2, D3, D4, D5, DS1	1N4007
12	2	Diode	D6, D7	1N4148
13	1	Coil	L1	330µH
14	1	Coil	L2	3.9µH
15	1	Resistor	R1	4.7kΩ , 1/4W, 5%
16	1	Resistor	R2	50Ω , 1/4W, 5%
17	1	Resistor	R3	2.4kΩ , 2W, 5%
18	1	Resistor	R4	1kΩ , 1/4W, 5%
19	1	Resistor	R5	2.2kΩ , 1/4W, 1%
20	1	Resistor	R6	2kΩ , 1/4W, 1%
21	1	Resistor	R7	5Ω , 1/4W, 5%
22	1	Resistor	R8	300Ω , 1/4W, 5%
23	1	Resistor	R9	150Ω , 1/4W, 5%
24	1	Resistor	R10	510Ω , 1/4W, 5%
25	3	Resistor	R11, R13, R14	3 Ω , 1/4W, 1%
26	1	Resistor	R12	27k Ω , 1/8W, 5%
27	2	Resistor	R15, R16	6kΩ , 1/8W, 5%
28	1	Resistor	RS2	200kΩ , 1/4W, 5%
29	1	Resistor	RS4	10Ω , 1/4W, 5%
30	1	Shunt Regulator	U1	TL431A
31	1	Control IC	U2	FSQ510
32	1	Opto-coupler	U3	PC817A
33	1	Transistor	Q1	KSP2222A
34	1	Thermister	THR1	10KD-5
35	1	Transformer	TX1	EE1616

Package Dimensions





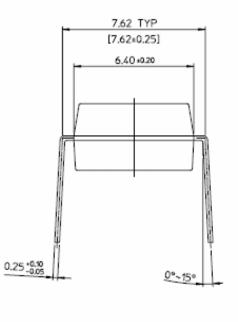


Figure 15. FSQ510 7-DIP

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UniFET™ UltraFET® VCX^{TM} Wire™

PRODUCT STATUS DEFINITIONS **Definition of Terms**

Datasheet Identification	Product Status	Definition
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