MC44604

High Safety Pulsed Mode Standby GreenLine™ PWM Controller

The MC44604 is an enhanced high performance controller that is specifically designed for off−line and dc−to−dc converter applications. Its high current totem pole output is ideally suited for driving a power MOSFET.

The MC44604 is an evolution of the MC44603A. Like the MC44603A, the MC44604 has been optimized to operate with universal ac mains voltage from 80 V to 280 V. It also offers enhanced safety and reliable power management thanks to its protection features (foldback, overvoltage detection, soft−start, accurate demagnetization detection).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a so−called pulsed mode standby operation of the converter, significantly reducing the converter consumption in standby mode.

Current Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle−by−Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft−Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine™ Controller™

- Low Start−Up and Operating Current
- Pulsed Mode Standby for Low Standby Losses
- Low dV/dT for Low EMI

Features

- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

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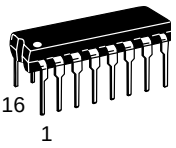
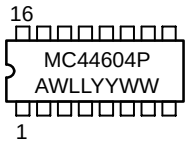
MARKING DIAGRAM

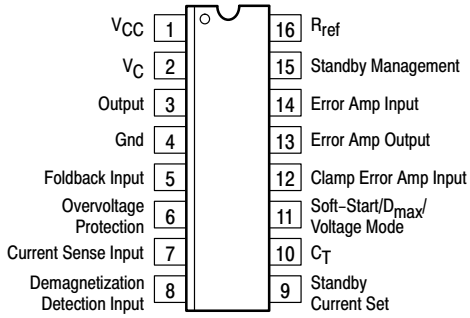


PDIP−16
P SUFFIX
CASE 648



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



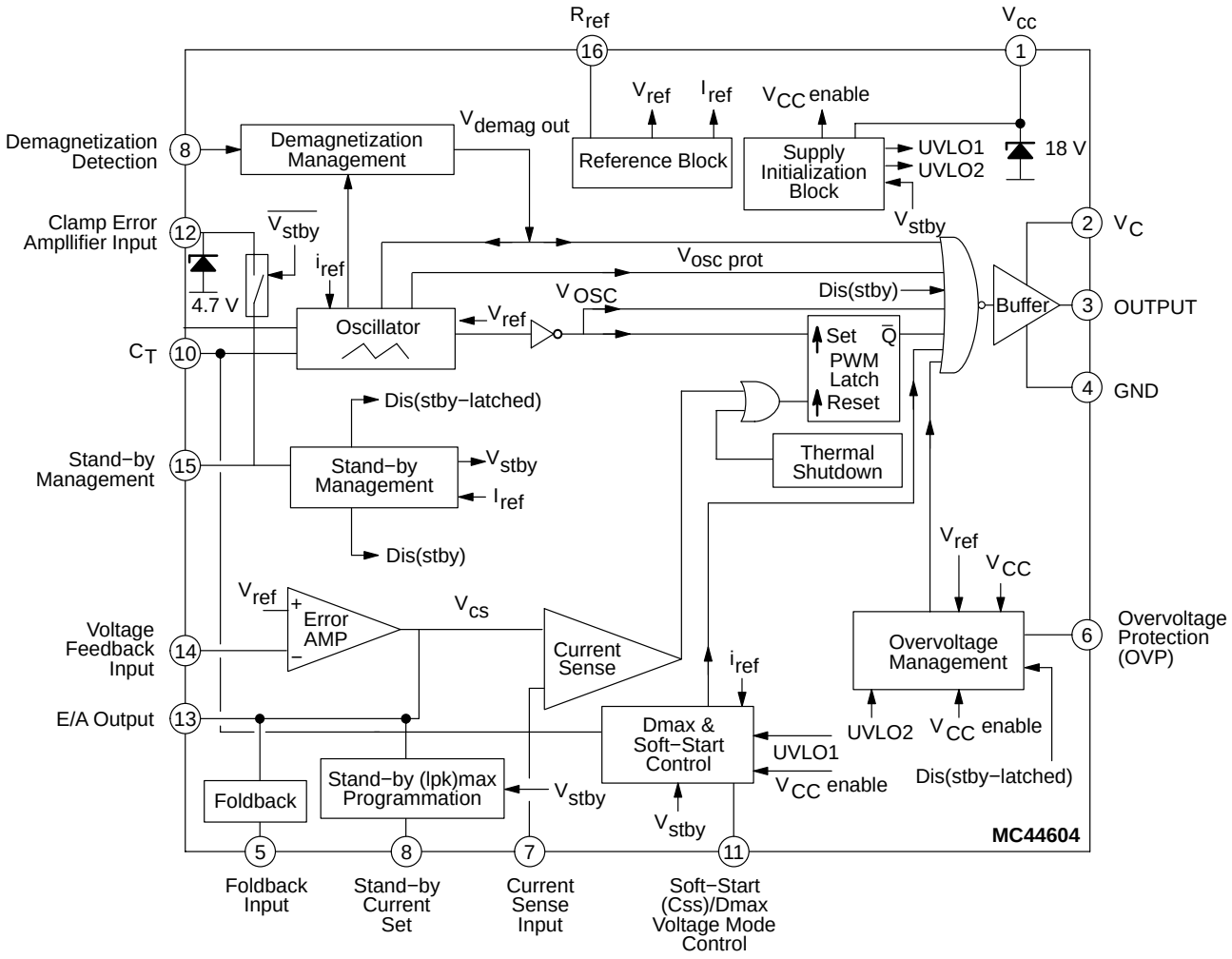
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
MC44604P	PDIP−16	25 Units/Rail
MC44604PG	PDIP−16 (Pb−Free)	25 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Block Diagram



MAXIMUM RATINGS

Rating	Pin #	Symbol	Value	Unit
Total Power Supply and Zener Current		$(I_{CC} + I_Z)$	30	mA
Output Supply Voltage with Respect to Ground	2 1	V_C V_{CC}	18	V
Output Current* Source Sink	3	 $I_{O(Source)}$ $I_{O(Sink)}$	 −750 750	mA
Output Energy (Capacitive Load per Cycle)		W	5.0	μJ
Soft−Start	11	V_{SS}	−0.3 to 2.2	V
Clamp Error Amp Input	12	V_{CLEA}	−0.3 to 4.5	V
Foldback Input, Stand−by Management			−0.3 to V_{CC} + 0.3	V
Overvoltage Protection, Current Sense Input, R_{ref}, Error Amp Input, Error Amp Output, C_T, Stand−by Current Set		V_{in}	−0.3 to 5.5	V
Demagnetization Detection Input Current Source Sink	8	 $I_{demag-ib\ (Source)}$ $I_{demag-ib\ (Sink)}$	 −4.0 10	mA
Error Amplifier Output Sink Current	13	$I_{E/A\ (Sink)}$	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation at T_A = 85°C Thermal Resistance, Junction−to−Air		 P_D $R_{\theta JA}$	 0.6 100	 W °C/W
Operating Junction Temperature		T_J	150	°C
Operating Ambient Temperature		T_A	−25 to +85	°C

*Maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 1], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C [Note 2], unless otherwise noted.)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION (Note 3)						
Output Voltage*	3					V
Low Level Drop Voltage (I_{Sink} = 100 mA)		V_{OL}	−	1.0	1.2	
(I_{Sink} = 500 mA)			−	1.4	2.0	
High Level Drop Voltage (I_{Source} = 200 mA)		V_{OH}	−	1.5	2.0	
(I_{Source} = 500 mA)			−	2.0	2.7	
Output Voltage During Initialization Phase	3	V_{OL}				V
V_{CC} = 0 to 1.0 V, I_{Sink} = 10 μA			−	−	1.0	
V_{CC} = 1.0 to 5.0 V, I_{Sink} = 100 μA			−	0.1	1.0	
V_{CC} = 5.0 to 13 V, I_{Sink} = 1.0 mA			−	0.1	1.0	
Output Voltage Rising Edge Slew−Rate (C_L = 1.0 nF, T_J = 25°C)	3	dVo/dT	−	300	−	V/μs
Output Voltage Falling Edge Slew−Rate (C_L = 1.0 nF, T_J = 25°C)	3	dVo/dT	−	−300	−	V/μs
ERROR AMPLIFIER SECTION						
Voltage Feedback Input ($V_{E/A\ out}$ = 2.5 V)	14	V_{FB}	2.4	2.5	2.6	V
Input Bias Current (V_{FB} = 2.5 V)	14	I_{FB-ib}	−2.0	−0.6	−	μA
Open Loop Voltage Gain ($V_{E/A\ out}$ = 2.0 V to 4.0 V)		A_{VOL}	65	70	−	dB
Unity Gain Bandwidth		BW				MHz
T_J = 25°C			−	−	−	
T_A = −25° to +85°C			−	−	5.5	
Voltage Feedback Input Line Regulation (V_{CC} = 10 V to 15 V)	14	$V_{FBline-reg}$	−10	−	10	mV

*V_C must be greater than 5.0 V.
1. Adjust V_{CC} above the start−up threshold before setting to 12 V.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. No output signal when the Error Amplifier is in Low State, i.e., V_{FB} = 2.7 V.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 1], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C [Note 2], unless otherwise noted.)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION (continued)						
Output Current	13					mA
Sink ($V_{E/A\ out}$ = 1.5 V, V_{FB} = 2.7 V)		I_{Sink}				
T_A = −25° to +85°C			2.0	12	–	
Source ($V_{E/A\ out}$ = 5.0 V, V_{FB} = 2.3 V)		I_{Source}				
T_A = −25° to +85°C			−2.0	–	−0.2	
Output Voltage Swing	13					V
High State ($I_{E/A\ out\ (source)}$ = 0.5 mA, V_{FB} = 2.3 V)		V_{OH}	5.5	6.5	7.5	
Low State ($I_{E/A\ out\ (sink)}$ = 0.33 mA, V_{FB} = 2.7 V)		V_{OL}	–	1.0	1.1	
REFERENCE SECTION						
Reference Output Voltage (V_{CC} = 10 V to 15 V)	16	V_{ref}	2.4	2.5	2.6	V
Reference Current Range ($I_{ref} = V_{ref}/R_{ref}$, R = 5.0 k to 25 kΩ)	16	I_{ref}	−500	–	−100	μA
Reference Voltage Over I_{ref} Range		ΔV_{ref}	−40	–	40	mV
OSCILLATOR SECTION						
Frequency		F_{OSC}				kHz
T_A = 0° to +70°C			40.5	46	48.5	
T_A = −25° to +85°C			40	–	49	
Frequency Change with Voltage (V_{CC} = 10 V to 15 V)		$\Delta F_{OSC}/\Delta V$	–	0.05	–	%/V
Frequency Change with Temperature (T_A = −25° to +85°C)		$\Delta F_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak−to−Peak)	10	$V_{OSC(P-P)}$	–	2.0	–	V
Ratio Charge Current/Reference Current (T_A = −25° to +85°C)		I_{charge}/I_{ref}	0.35	–	0.43	–
Fixed Maximum Duty Cycle = $I_{discharge}/(I_{discharge} + I_{charge})$		D	78	80	82	%
UNDERVOLTAGE LOCKOUT SECTION						
Start−up Threshold	1	$V_{stup-th}$	13.6	14.5	15.4	V
Disable Voltage After Threshold Turn−On	1	$V_{disable1}$				V
T_A = 0° to +70°C			8.6	9.0	9.4	
T_A = −25° to +85°C			8.3	–	9.6	
Disable Voltage After Threshold Turn−On	1	$V_{disable2}$	7.0	7.5	8.0	V
Delta V_{CC} During Standby ($V_{stup-th}$ −$V_{disable2}$) (T_A = −25°C to 85°C)	1	$V_{stup-th}$ −$V_{disable2}$	1.8	2.0	2.2	V
DEMAGNETIZATION DETECTION SECTION						
Demagnetization Detect Input	8					
Demagnetization Comparator Threshold (V_{pin8} Decreasing)		$V_{demag-th}$	50	65	80	mV
Propagation Delay (Input to Output, Low to High)		–	–	0.25	–	μs
Input Bias Current (V_{demag} = 65 mV)		$I_{demag-Ib}$	−0.5	–	–	μA
Negative Clamp Level (I_{demag} = −2.0 mA)		$C_{L(neg)}$	–	−0.38	–	V
Positive Clamp Level (I_{demag} = +2.0 mA)		$C_{L(pos)}$	–	0.72	–	V
SOFT−START SECTION						
Ratio Charge Current/I_{ref}		$I_{ss(ch)}/I_{ref}$				–
T_A = 0° to +70°C			0.37	0.4	0.43	
T_A = −25° to +85°C			0.36	–	0.44	
Discharge Current ($V_{soft-start}$ = 1.0 V)	11	$I_{discharge}$	1.5	5.0	–	mA
Clamp Level		$V_{ss(CL)}$	2.2	2.4	2.6	V
Duty Cycle ($R_{soft-start}$ = 12 kΩ)		$D_{soft-start\ 12k}$	36	42	49	%
($V_{soft-start\ (pin11)}$ = 0.1 V)		$D_{soft-start}$	–	–	0	

1. Adjust V_{CC} above the start−up threshold before setting to 12 V.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 1], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = −25° to +85°C [Note 2], unless otherwise noted.)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION						
Maximum Current Sense Input Threshold ($V_{Feedback\ (pin14)}$ = 2.3 V and $V_{foldback\ (pin6)}$ = 1.2 V)	7	V_{cs-th}	0.93	0.96	1.00	V
Input Bias Current	7	I_{cs-ib}	−10	−2.0	−	μA
Propagation Delay* in Normal Mode in Standby Mode		t_{CS-NM} $t_{CS-stby}$	− −	120 120	200 200	ns
OVERVOLTAGE SECTION						
Protection Threshold Level on V_{OVP}	6	V_{OVP-th}	2.42	2.5	2.58	V
Propagation Delay (V_{OVP} > 2.58 V to V_{out} Low)			1.0	−	3.0	μs
Protection Level on V_{CC} T_A = 0° to +70°C T_A = −25° to +85°C		$V_{CC\ prot}$	 16.1 15.9	 17 −	 17.9 18.1	V
Input Resistance T_A = 0° to +70°C T_A = −25° to +85°C		−	 1.5 1.4	 2.0 −	 3.0 3.4	kΩ
FOLDBACK SECTION (Note 3)						
Current Sense Voltage Threshold ($V_{foldback\ (pin5)}$ = 0.9 V)	5	V_{cs-th}	0.84	0.88	0.89	V
Foldback Input Bias Current ($V_{foldback\ (pin5)}$ = 0 V)	5	$I_{foldback-Ib}$	−6.0	−2.0	−	μA
CLAMP ERROR AMPLIFIER INPUT						
Clamp Level (@ I = 30 mA)	12	Vcl	4.5	4.7	4.9	V
STANDBY PULSED MODE SECTION						
Standby Initialization Current Ratio (S1 closed)	15	I_{init}/I_{ref}	126	140	154	−
Minimum Initialization Current Pulse Width*		T_{init}	−	−	1.0	μs
Standby On Detection Current Ratio	15	I_{det}/I_{ref}	0.34	0.38	0.42	−
Standby Regulation Current Ratio	15	I_{reg}/I_{ref}	18	20.5	23	−
Standby Bias Current (S1 and S2 open; 0 V < V_{pin15} < $V_{stup-th}$)**	15	$I_{stby-ib}$	−1.0	−	2.0	μA
STANDBY CURRENT SET						
Peak Standby Current Setting Ratio T_A = 0° to +70°C T_A = −25° to +85°C	9	 $I_{pk-stby}/I_{ref}$ −	 0.37 0.36	 0.4 0.4	 0.43 0.44	−
Standby Current Sense Threshold Ratio*	7	V_{pin9}/V_{cs-st}	2.4	2.6	2.9	−
TOTAL DEVICE						
Power Supply Current Startup* Operating T_A = −25° to +85°C (Note 2)		I_{CC}	 − 16	 0.3 20	 0.45 24	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)		V_Z	18.5	−	−	V
Thermal Shutdown		−	−	155	−	°C

* This is the minimum time during which the pin 15 current must be higher than I_{init} to enable the detection of the transition normal to standby mode.
**Tested using V_{CC} = 6.0 V, 9.0 V, 13.5 V, the MC44604 being off.

*Tested using V_{pin9} = 0.2 V, 0.4 V, 0.6 V, 0.8 V, 1.0 V.

*Tested using V_{CC} = 6.0 V, 9.0 V, 13.5 V, the MC44604 being off.

1. Adjust V_{CC} above the start−up threshold before setting to 12 V.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. This function can be inhibited by connecting pin 5 to V_{CC}.

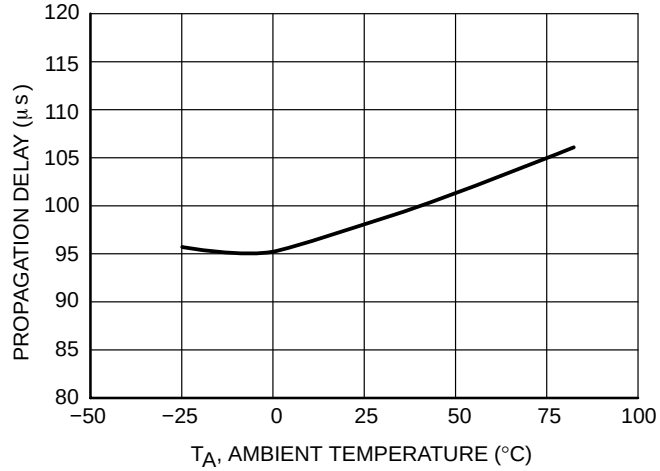


Figure 1. Propagation Delay Current Sense Input vs. Temperature

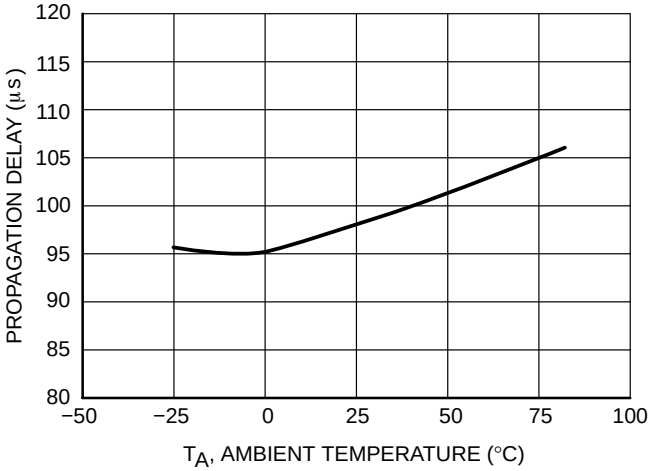


Figure 2. Propagation Delay Current Sense Input in Standby vs. Temperature

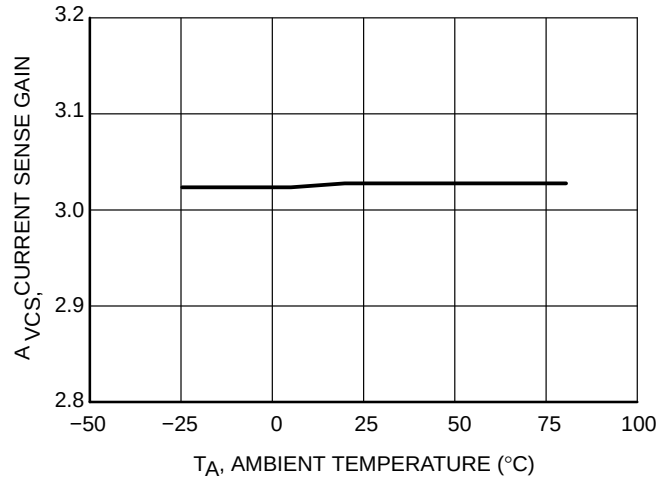


Figure 3. Current Sense Gain vs. Temperature

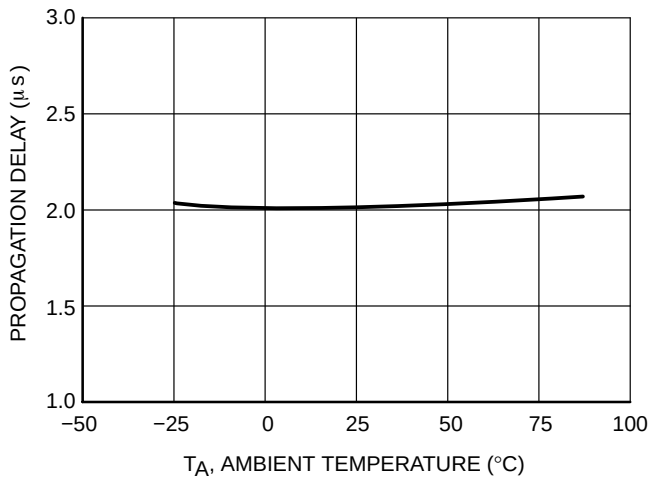


Figure 4. Propagation Delay Current (V_{ovp} > 2.58 V to V_{out} Low) vs. Temperature

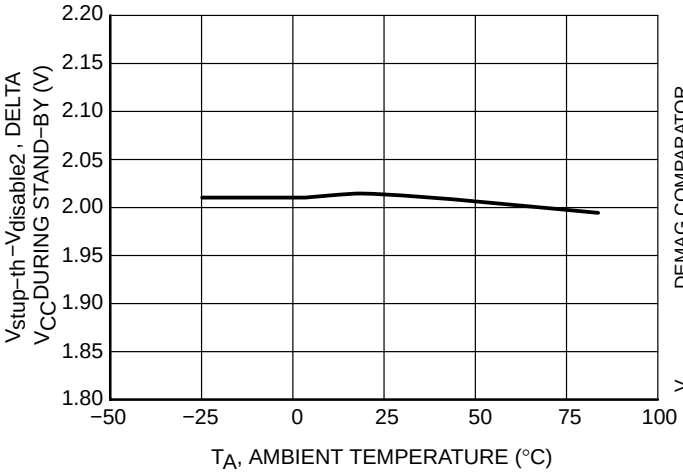


Figure 5. Delta V_{CC} During Standby

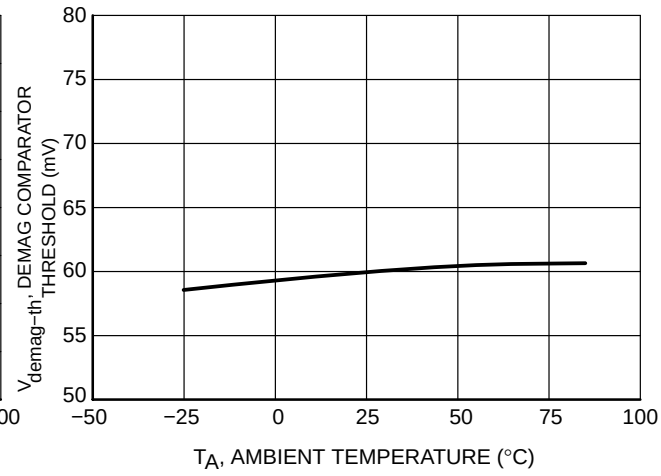


Figure 6. Demag Comparator Threshold vs. Temperature

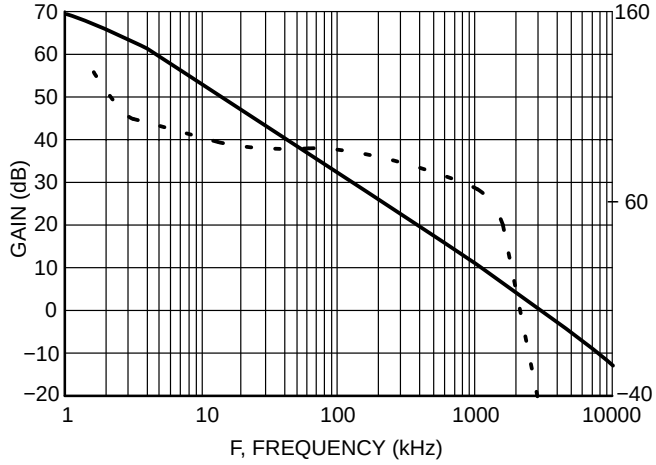


Figure 7. Error Amplifier Gain and Phase vs. Frequency

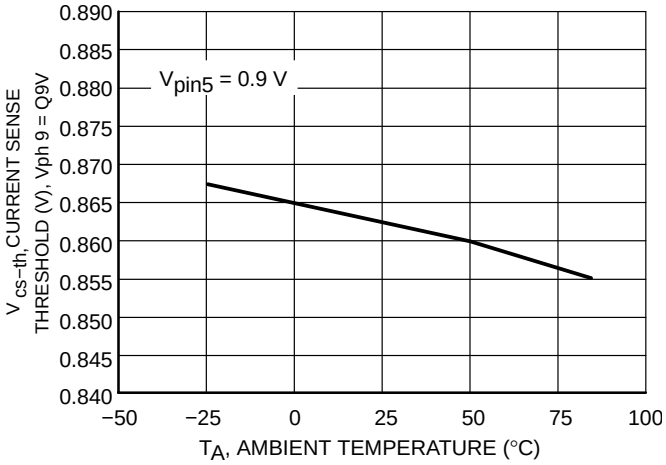


Figure 8. Current Sense Voltage Threshold vs. Temperature

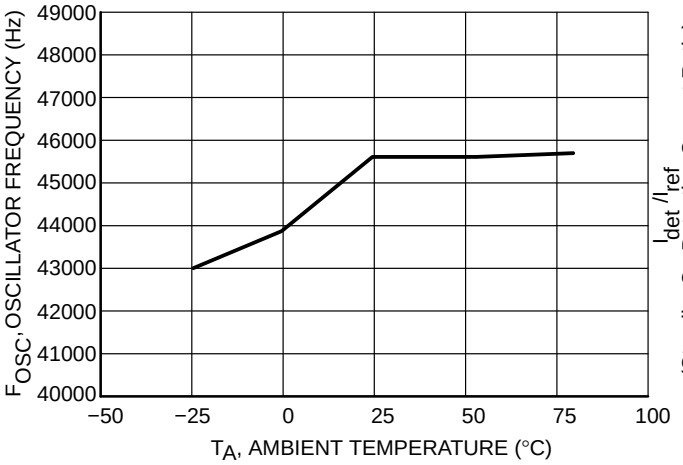


Figure 9. Oscillator Frequency vs. Temperature

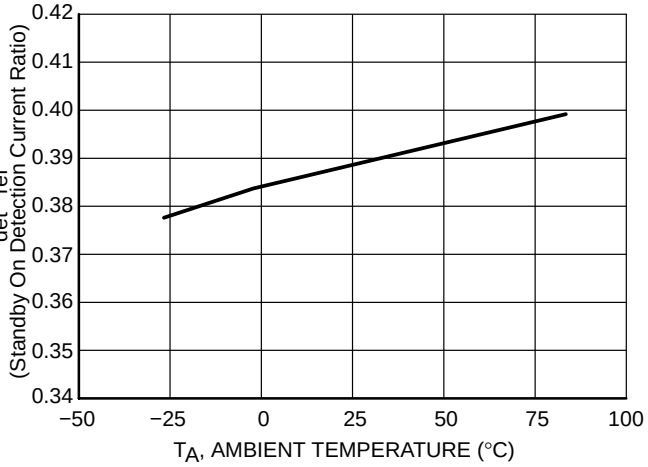


Figure 10. Standby On Detection Current Ratio vs. Temperature

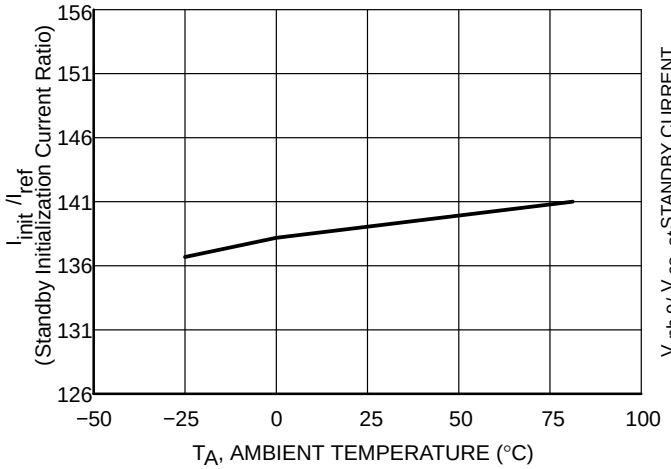


Figure 11. Standby Initialization Current Ratio vs. Temperature

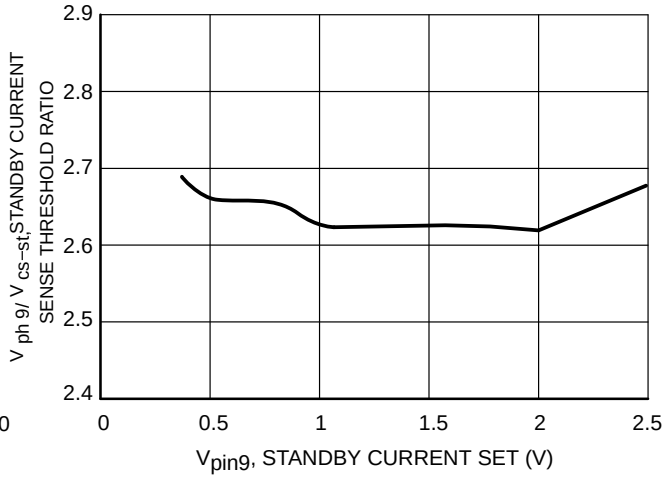


Figure 12. Standby Current Sense Threshold Ratio

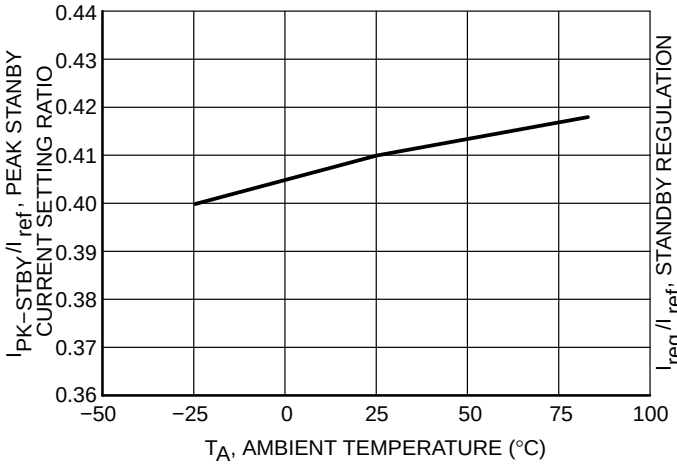


Figure 13. Peak Standby Current Setting Ratio vs. Temperature

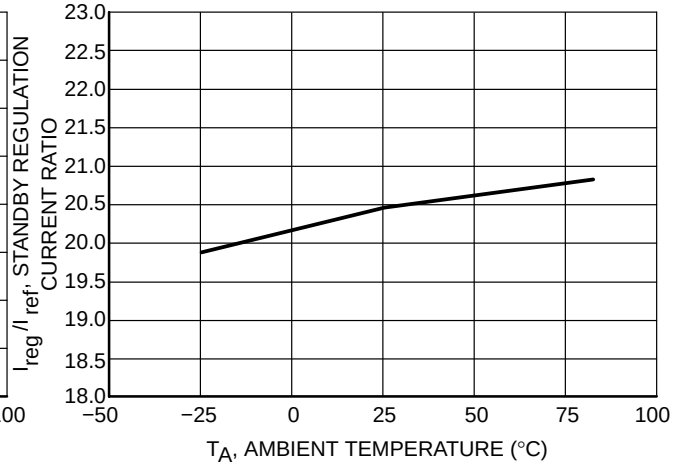


Figure 14. Standby Regulation Current Ratio vs. Temperature

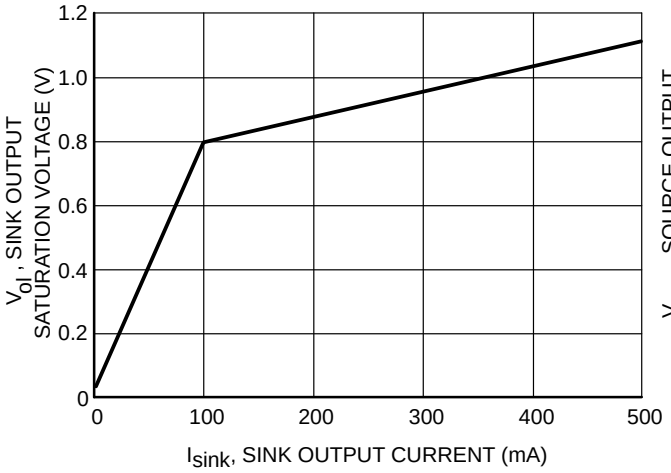


Figure 15. Sink Output Saturation Voltage vs. Sink Current

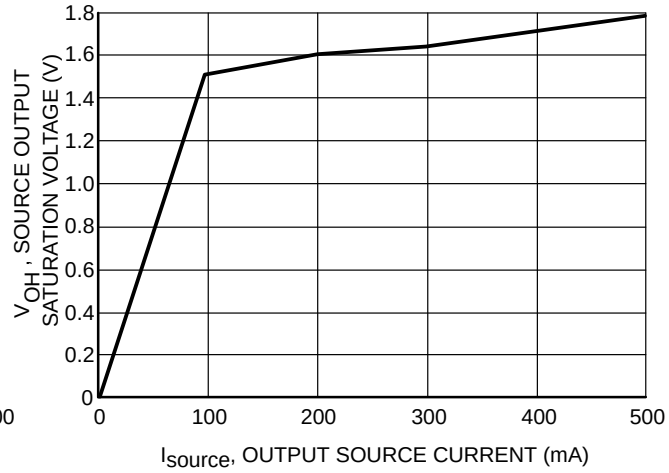


Figure 16. Source Output Saturation Voltage vs. Source Current

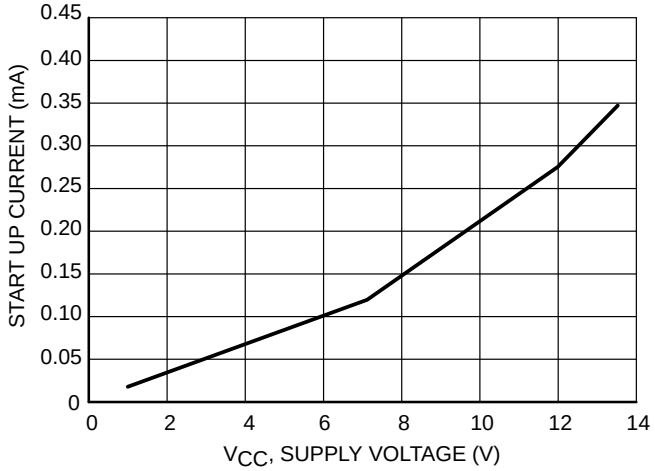


Figure 17. Start−up Current vs. V_{CC}

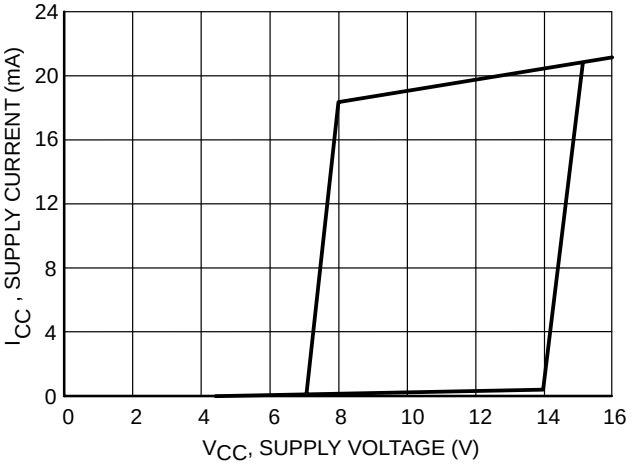


Figure 18. Supply Current vs. Supply Voltage

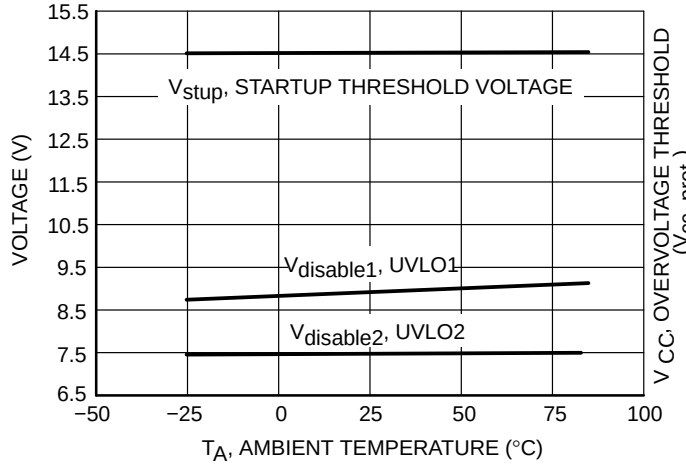


Figure 19. Start−up Threshold, UVLO1, UVLO2 Voltage vs. Temperature

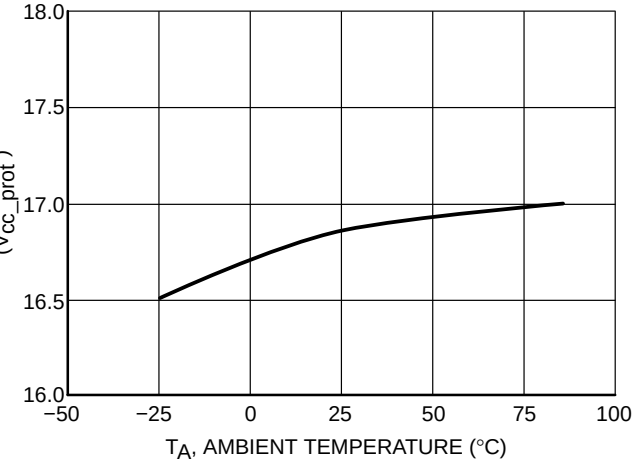


Figure 20. Protection Level on V_{CC} vs. Temperature

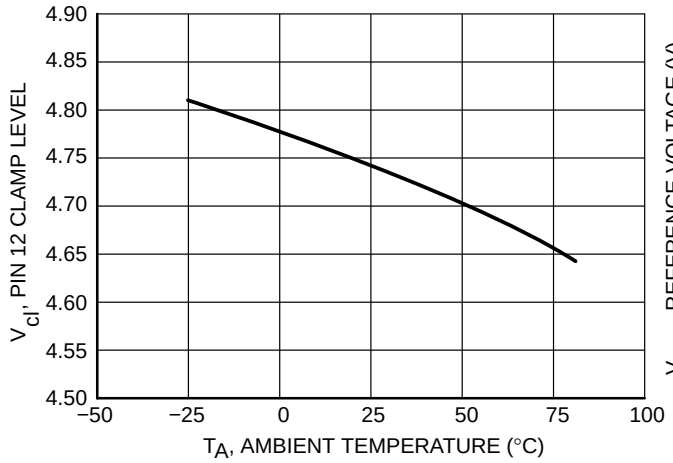


Figure 21. Clamp Error Amplifier Input vs. Temperature

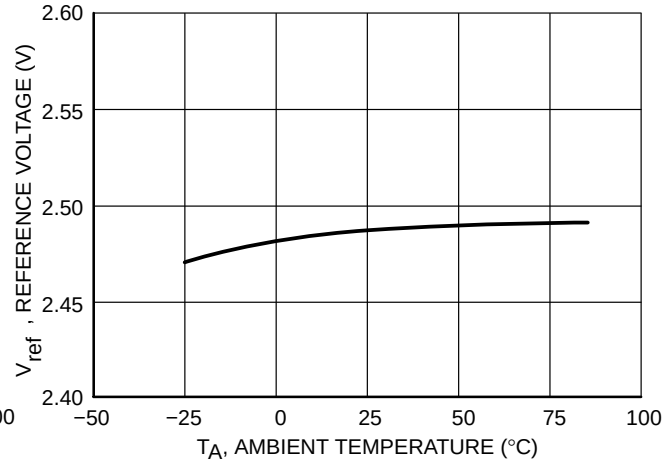


Figure 22. Reference Voltage vs. Temperature

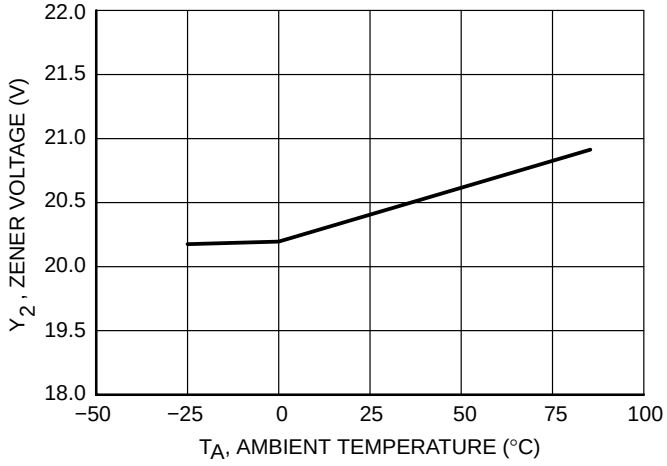


Figure 23. Power Supply Zener Voltage vs. Temperature

Pin	Name	Pin Description
1	V_{CC}	This pin is the positive supply of the IC.
2	V_C	The output high state, V_{OH}, is set by the voltage applied to this pin. With a separate connection to the power source, it gives the possibility to set by means of an external resistor the output source current at a different value than the sink current.
3	Output	The output current capability is suited for driving a power MOSFET. A Bipolar transistor can also be driven for low power applications. The maximum on−time of the duty cycle can last up to 80% of the switching period.
4	Gnd	The ground pin is a single return typically connected back to the power source, it is used as control and power ground.
5	Foldback Input	The foldback function ensures an overload protection. Feeding the foldback input with a portion of the V_{CC} voltage (1 V max) establishes on the system control loop a foldback characteristic allowing a smoother start−up and a sharper overload protection. The foldback action performs an active current sense clamping reduction. Above 1 V the foldback input is no more active.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 17 V the device gets disabled and requires a complete restart sequence. The overvoltage level is programmable.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when operating in current mode. A maximum level of 1 V allows to limit the inductor current either in current or voltage mode of operation.
8	Demagnetization Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback energy reservoir. A zero voltage detection corresponds to a complete core demagnetization. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to GND.
9	Standby Current Set	Using an external resistor connected to this pin, the standby burst mode peak current can be adjusted.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor C_T choice together with the R_{ref} resistance value. C_T, connected between pin 10 and GND, generates the oscillator sawtooth.
11	Soft−Start/D_{max}/Voltage−Mode	A capacitor or a resistor or a voltage source connected to this pin can temporary or permanently control the effective switching duty−cycle. This pin can be used as a voltage mode control input. By connecting pin 11 to Ground, the MC44604 can be shut down.
12	Clamp Error Amplifier Input	In normal mode, the current drawn from this pin, is used by the Error Amplifier to perform the regulation. A 4.7 V zener diode clamps the voltage of this pin.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It uses a voltage that is built up using the current drawn from the pin 12.
15	Standby Management	This block is designed to detect the standby mode. It particularly determines if the circuit must work in standby or in normal mode at each start−up. For that, it uses an information given by an external arrangement consisting of an opto−coupler. In standby mode, this block makes the circuit work in the standby configuration, and the current injected in the pin 15 is used to perform the regulation. In normal mode, this pin is internally connected to the pin 12.
16	R_{REF}	The R_{REF} values fixes the internal reference current which is used to perform the precise oscillator waveform. The current range goes from 100 μA up to 500 μA.

Operating Description Schematics

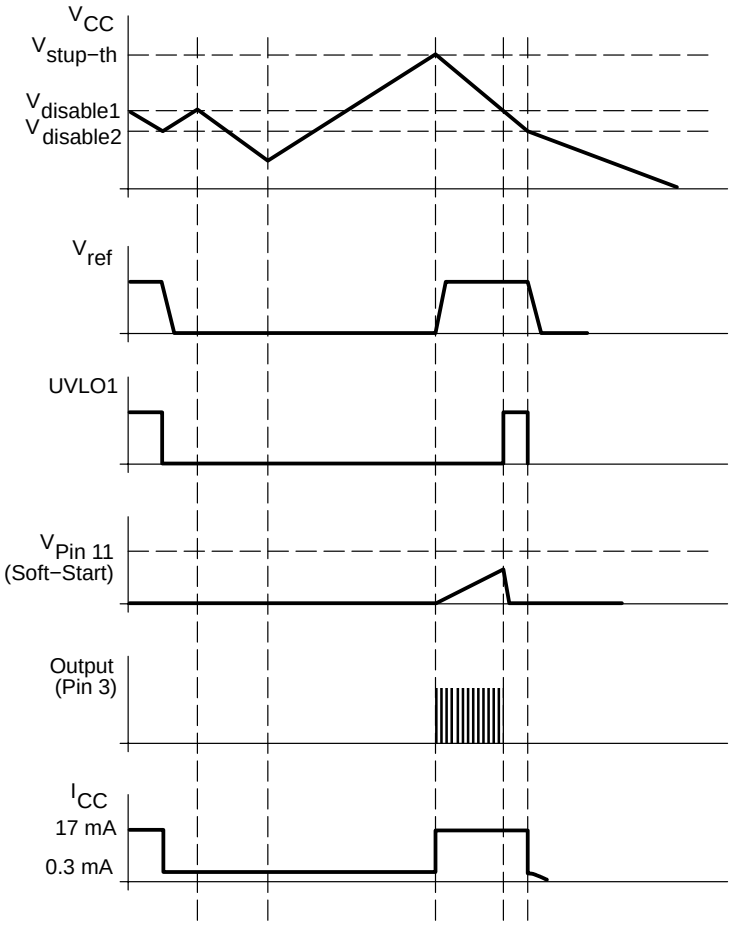


Figure 24. Switching Off Behavior

Operating Description Schematics

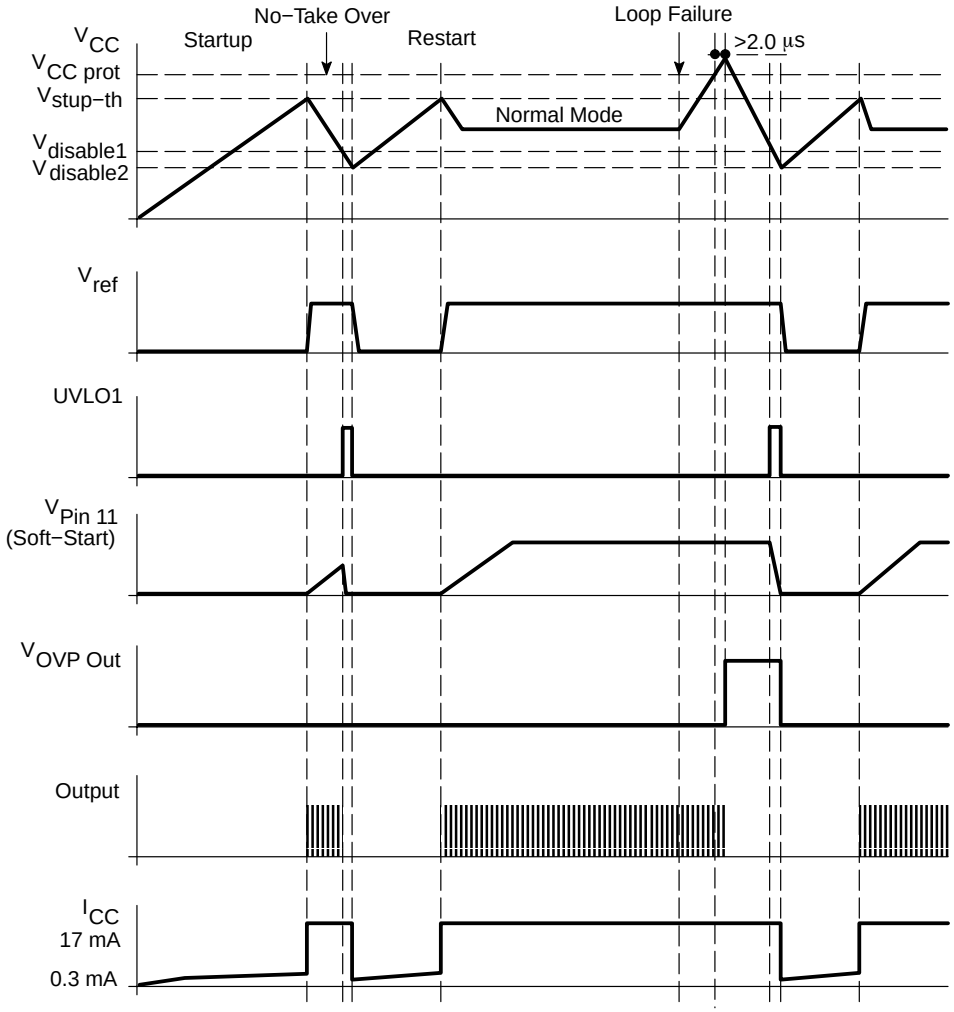


Figure 25. Starting Behavior and Overvoltage

Operating Description Schematics

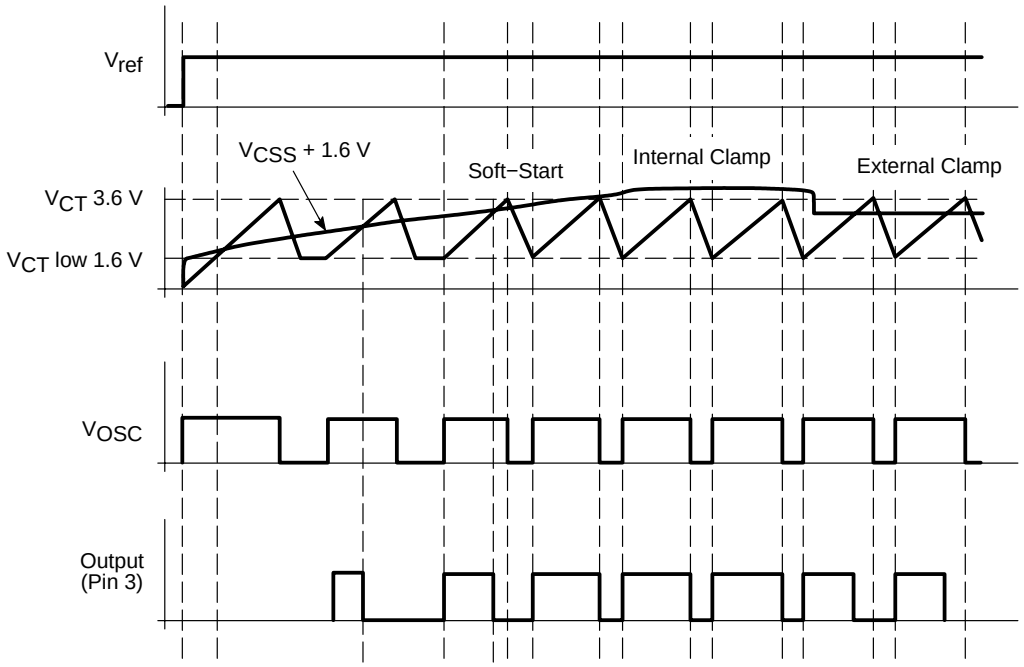


Figure 26. Soft−Start and D_{max}

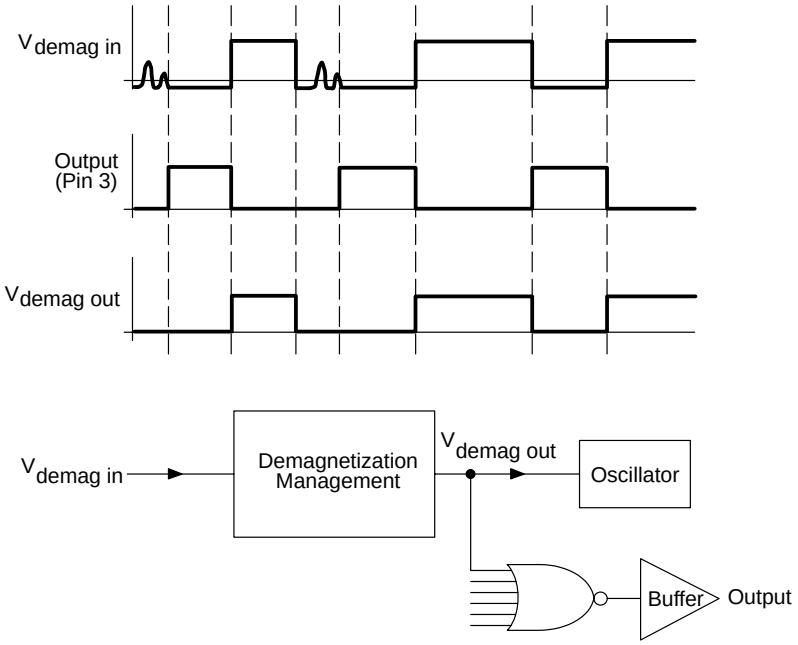


Figure 27. Demagnetization

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 70 dB. The non−inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is −2.0 μA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diodes drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 3) when Pin 13 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.2 mA) and the required output voltage (V_{OH}) to reach the current sense comparator's 1.0 V clamp level:

$$R_{f\,(min)} \approx \frac{3 \cdot 0(1 \cdot 0\ V) + 1 \cdot 4\ V}{0 \cdot 2\ mA} = 22\ k\Omega$$

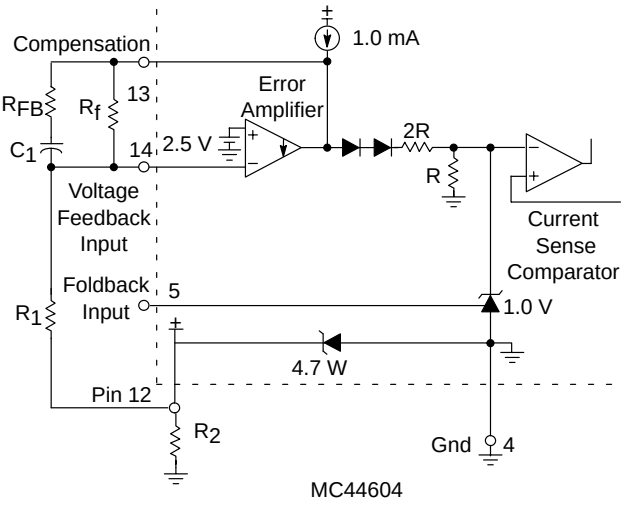


Figure 28. Error Amplifier Compensation

In a preferred embodiment, the feedback signal (current) is drawn from the pin 12 that is connected to the pin 15 in normal mode (Note 1). Using a resistor connected on pin 12, this current generates a voltage that is the input signal of the error amplifier arrangement.

Note 1. The error amplifier is not used in the standby mode regulation.

Current Sense Comparator and PWM Latch

The MC44604 can operate as a current mode controller and/or as a voltage mode controller. In current mode operation, the MC44604 uses the current sense comparator, where the output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 13). Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the power switch Q1.

In normal mode, this voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$I_{pk} \approx \frac{V_{(pin13)} - 1 \cdot 4\ V}{3\ R_S}$$

The Current Sense Comparator threshold is internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1 \cdot 0\ V}{R_S}$$

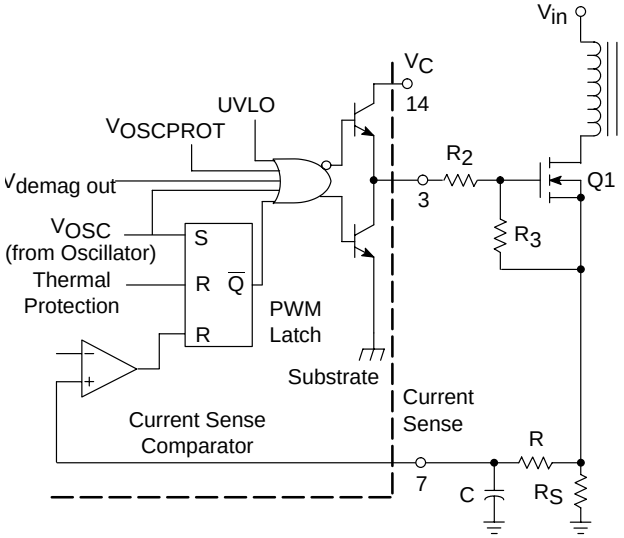


Figure 29. Output Totem Pole

Oscillator

The oscillator is a very accurate sawtooth generator.

The Sawtooth Generation

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V.

Indeed, the sawtooth is obtained by charging and discharging an external capacitor C_T (Pin 10), using two distinct current sources = I_{charge} and $I_{discharge}$. In fact, C_T is permanently connected to the charging current source (0.4 I_{ref}) and so, the discharge current source has to be higher than the charge one to be able to decrease the C_T voltage. This condition is performed, its value being (2 I_{ref}).

Two comparators are used to generate the sawtooth. They compare the C_T voltage to the oscillator valley and peak values. The comparison to the low value enables to detect the end of the discharge phase while the comparison to the high value determines when the charge cycle must be stopped. A latch (L_{DISCH}) memorizes the oscillator state.

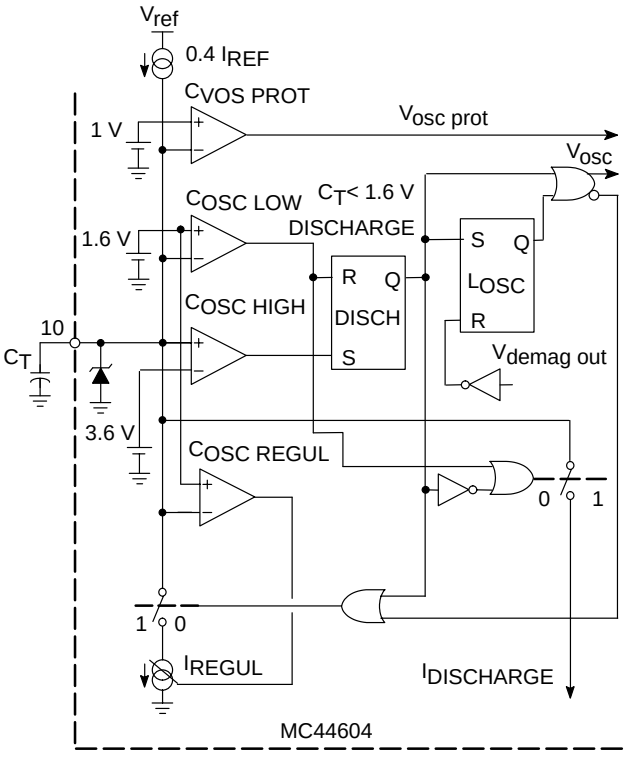


Figure 30. Oscillator

Now, in addition to the charge and discharge cycles, a third state can exist. This phase can be produced when at the end of the discharge phase, the oscillator has to wait for a demagnetization pulse before re−starting. During this delay, the C_T voltage must remain equal to the oscillator valley value (~1.6 V). So, a third regulated current source I_{REGUL} controlled by $C_{OSCREGUL}$, is connected to C_T in order to perfectly compensate the (0.4 I_{ref}) current source that permanently supplies C_T.

On−time is only allowed during the oscillator capacitor charge. So, the maximum duty cycle is 80%. (Note 1)

The demagnetization condition is taken into account by a second latch (L_{osc}). (Refer to demagnetization § for further details.)

Oscillator Frequency

The oscillator frequency can be deducted using the following equations:

$$T_{charge} = C_T \cdot \Delta V / I_{charge}$$

$$T_{discharge} = C_T \cdot \Delta V / I_{discharge}$$

where:

T_{charge} is the oscillator charge time

ΔV is the oscillator peak to peak value

I_{charge} is the oscillator charge current

and

$T_{discharge}$ is the oscillator discharge time

$I_{discharge}$ is the oscillator discharge current

So, as:

$f_{osc} = 1 / (T_{charge} + T_{discharge})$ if the REGUL arrangement is not activated, the following equation can be obtained:

$$f_{osc} \sim \frac{0.395}{R_{ref} \cdot C_T}$$

Demagnetization Block (Note 2)

To enable the output, the L_{osc} latch complementary output must be low. Now, this latch reset is activated by the L_{DISCH} output during the discharge phase. So, to restart, the L_{osc} has to be set (refer to Figure 30). To perform this, the demagnetization signal must be low.

In a fly−back, a good means to detect the demagnetization consists in using the V_{CC} winding voltage. Indeed this voltage is:

- negative during the on−time,
- positive during the off−time,
- equal to zero for the dead−time with generally a ringing (refer to Figure 31).

That is why, the MC44604 demagnetization detection consists of a comparator that can compare the V_{CC} winding voltage to a reference that is typically equal to 65 mV.

Note 1. The output is disabled by the signal $V_{osc\ prot}$ when V_{CT} is lower than 1 V. (Refer to Figure 29 and Figure 30.)

Note 2. The demagnetization detection can be inhibited by connecting pin 8 to the ground.

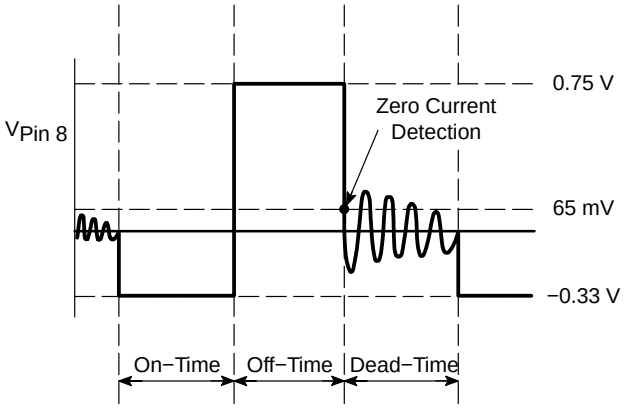


Figure 31. Demagnetization Detection

A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically −0.33 V. This negative clamp level is sufficient to avoid the substrate diode switching on.

In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 33). This process avoids that any ringing on the signal used on the pin 8, disrupts the demagnetization detection. Finally, this method results in a very accurate demagnetization detection.

For a higher safety, the demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 29).

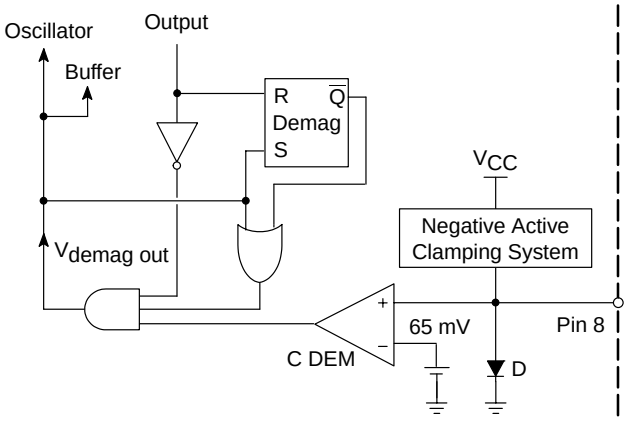


Figure 32. Demagnetization Block

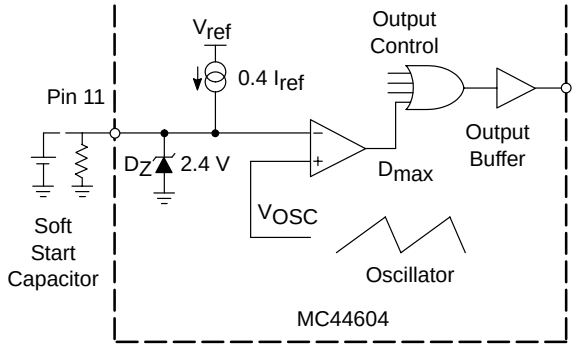


Figure 33. D_{max} and Soft−Start Block Diagram

Maximum Duty Cycle and Soft−Start Control

As explained in the paragraph “oscillator”, the duty cycle cannot be more than 80%. Now, using the D_{max} and soft−start control, this duty cycle can be limited to a lower value. Indeed as depicted in Figure 34, the pin 11 voltage is compared to the oscillator sawtooth, so that the MC44604 output should be disabled as soon as the pin 11 level becomes lower than the oscillator voltage (refer to Figure 27 and to Figure 25).

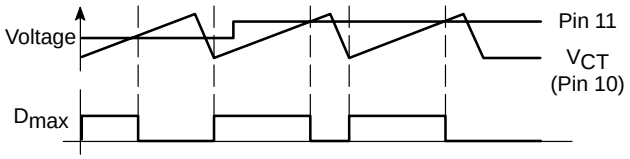


Figure 34. Maximum Duty Cycle Control

Now, using the internal current source (0,4 I_{ref}), the pin 11 voltage can easily be fixed by connecting a resistor to this pin.

If a capacitor is connected to pin 11 (without any resistor or in parallel to a resistor for instance), the pin 11 voltage increases from 0 to its maximum value progressively (refer to Figure 26).

Thus, the allowed maximum duty cycle grows for a delay depending on the capacitor value (and the resistor value when a resistor is connected).

So, this pin can be used to limit the duty cycle during the start−up phase and thus, to perform a soft−start.

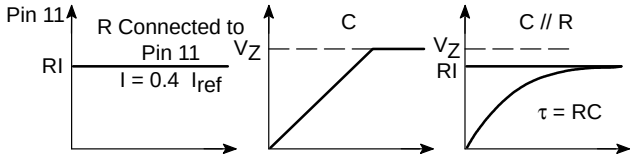


Figure 35. Different Possible Uses of Pin 11

In any case (particularly if no external component is connected to pin 11), an internal zener diode (D_Z, refer to Figure 34) is able to clamp the pin 11 voltage to a value V_Z that is higher than the oscillator value and so, that results in no max duty cycle limitation.

As soon as $V_{disable1}$ is detected, a signal UVLO1 is generated until the V_{CC} voltage falls down to $V_{disable2}$ (refer to the undervoltage lockout section paragraph). During the delay between the disable 1 and the disable 2, using a transistor controlled by UVLO1, the pin 11 voltage is made equal to zero in order to make the max duty cycle and soft−start arrangement ready to work for the next restart.

In standby mode, this block is inhibited in order not to interfere with the Standby Current Set.

Protection

The MC44604 can ensure a high converter reliability thanks to the protection it offers.

Demagnetization Detection (Refer to Demag §)

Foldback

As depicted in Figure 28, the foldback input (pin 5) enables to reduce the maximum V_{CS} value that would be equal to 1 typically, if there was no foldback action. Finally, the foldback arrangement is a programmable peak current limitation.

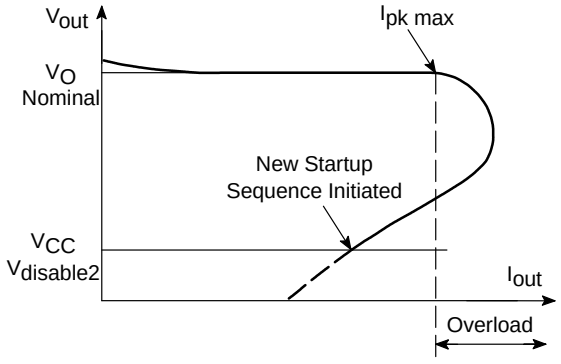


Figure 36. Foldback Characteristic

It could be used as a soft−start (by connecting to pin 5, a gradually increasing voltage) but in fact, it has been designed to provide the system with an effective overload protection.

Indeed, as the output load gradually increases, the required converter peak current becomes higher and so, V_{CS} grows up till it reaches its maximum value (normally, $V_{CS\ max}$ = 1 V).

Then if the output load keeps on increasing, the system is not able to supply enough energy to maintain the output regulation. Consequently, the decreasing output can be used to apply a voltage that diminishes to a value lower than 1 V, to pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic is obtained (refer to Figure 36).

The foldback action can be inhibited by connecting the pin 5 to V_{CC}.

Overvoltage Protection

The overvoltage arrangement consists of a comparator that compares the pin 6 voltage to V_{ref} (2,5 V) (refer to Figure 37).

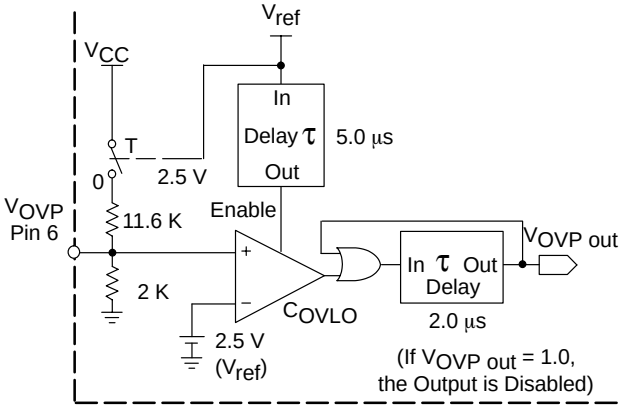


Figure 37. Overvoltage Protection

If no external component is connected to pin 6, the comparator non inverting input voltage is nearly equal to:

$$\left(\frac{2\ k\Omega}{11,6\ k\Omega + 2\ k\Omega}\right) \bullet V_{CC}$$

So, the comparator output is high when:

$$\left(\frac{2\ k\Omega}{11,6\ k\Omega + 2\ k\Omega}\right) \bullet V_{CC} \geq 2,5\ V$$

$$V_{CC} \geq 17\ V$$

A delay latch (2 μs) is incorporated in order to only take into account the overvoltages that last at least 2 μs.

If this condition is achieved, V_{OVPout} the delay latch output becomes high and as this level is brought back to the input through an OR gate, V_{OVPout} remains high (and so, the IC output is disabled) until V_{ref} is disabled.

Consequently when an overvoltage longer than 2 μs is detected, the output is disabled until a new circuit restart.

The V_{CC} is connected when once the circuit has started−up in order to limit the circuit start−up consumption (T is switched on when once V_{ref} has been generated).

The overvoltage section is enabled 5 μs after the regulator has started to allow the reference V_{ref} to stabilize.

By connecting external resistors to pin 6, the threshold V_{CC} level can be changed.

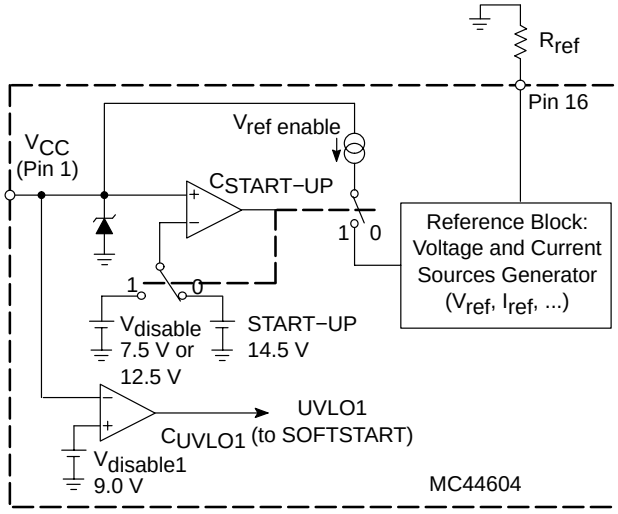


Figure 38. V_{CC} Management

Undervoltage Lockout Section

As depicted in Figure 39, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing operation of the system.

Indeed, the V_{CC} is connected to the non inverting input of a comparator that has an upper threshold equal to 14,5 V ($V_{stup-th}$) and a lower one equal to 7.5 V ($V_{disable2}$) in normal mode and 14.5 V and 12.5 V in Standby mode (typical values) (Note 1).

This hysteresis comparator enables or disables the reference block that generates the voltage and current sources required by the system.

This block particularly, produces V_{ref} (pin 16 voltage) and I_{ref} that is determined by the resistor R_{ref} connected between pin 16 and the ground:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} \text{ where } V_{ref} = 2.5 \text{ V (typically)}$$

In addition to this, V_{CC} is compared to a second threshold level that is nearly equal to 9 V ($V_{disable1}$) so that in normal mode, a signal UVLO1 is generated to reset the maximum duty cycle and soft−start block and so, to disable the output stage (refer to Max. Duty Cycle and Soft−Start §) as soon as V_{CC} becomes lower than $V_{disable1}$. In this way, the circuit is reset and made ready for a next start−up, before the reference block is disabled (refer to Figure 26). In standby, UVLO1 is not active (there is no need to discharge the soft−start capacitor as the soft−start pin is maintained short circuited).

Note 1. In standby the difference between $V_{disable2}$ and $V_{stup-th}$ is decreased not to have too low pulsed mode frequencies.

Thus, finally in normal mode, the upper V_{CC} limit that enables the output to be active, is 9.4 V (maximum value of $V_{disable1}$) and so the minimum hysteresis is 4.2 V. [$(V_{stup-th})_{min}$ = 13.6 V].

The large hysteresis and the low start−up current of the MC44604 make it ideally suited for off−line converter applications where efficient bootstrap start−up techniques are required.

Standby Management

The MC44604 has been designed to detect the transitions between the standby and normal mode and to manage each mode in an optimal way.

In standby, the device monitors a pulsed mode that enables to drastically reduce the power consumption.

Pulsed Mode

The MC44604 standby is preferably associated to a flyback configuration as depicted in Figure 39.

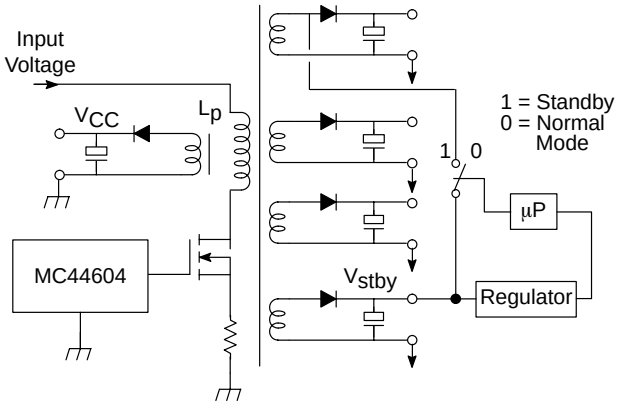


Figure 39. Standby Flyback Configuration

In effect, by this means, all the output regulation levels are divided by the ratio:

$$\frac{V_{HV}}{V_{stby}}$$

where V_{HV} is the normal mode high voltage regulation level, V_{stby} is the standby μP supply voltage.

For instance, in the case of TV or monitors applications, the output levels (except the μP supply voltage, V_{stby}) are drastically reduced by a ratio in the range of 10.

Consequently, as the output voltages are reduced, the losses due to the output leakage consumption, are practically eliminated, without having to disconnect the loads.

Start−up Operations

The choice of the right configuration (normal or standby) is performed at each start−up.

That is why, as explained in the transitions §, at each change of mode, the MC44604 is first turned off so that a new start−up should be performed.

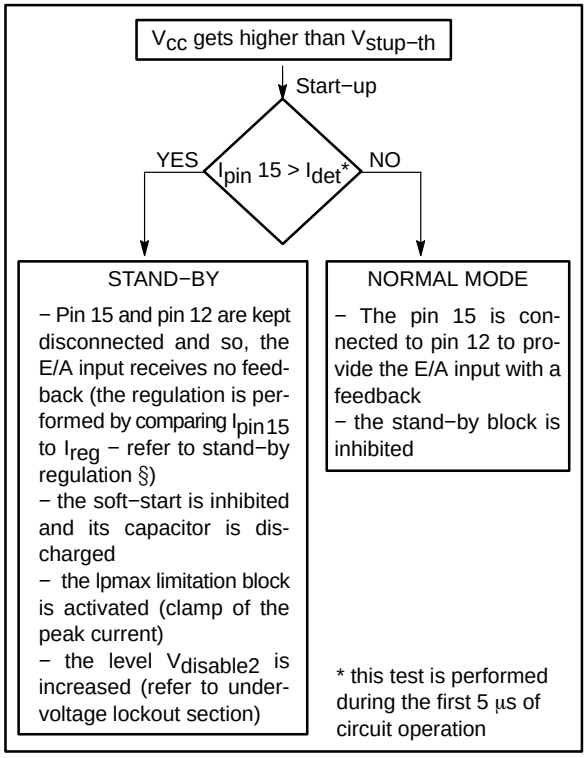


Figure 40. Start−up Operation

At each start−up, the circuit detects if it must work in standby or in normal mode configuration.

To do that, the circuit compares the current I_{pin15} to I_{det} so that, if:

- $I_{pin15} > I_{det}$: Standby mode
- $I_{pin15} < I_{det}$: Normal mode

According to the detected mode, the circuit configuration is set (refer to Figure 40).

This detection phase takes place during the first 5 μs of circuit operation in order to have the internal signals well stabilized before the decision is taken.

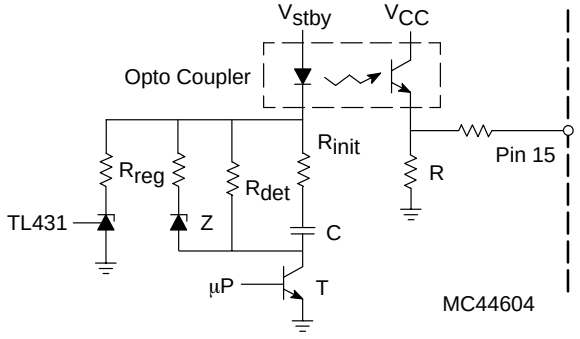


Figure 41. Standby Pin 15 Arrangement

Standby Management

The standby operation consists of two main phases:

- the **off phase** during which the MC44604 is off. During this sequence, the circuit V_{CC} is being charged and no energy is transferred to the output.
- the **active phase** during which the MC44604 is on. At this moment, some power can be drawn from the mains.

During the active phase, the power conversion is controlled so that:

- the normal mode regulation means (error amplifier) and the soft−start are inhibited
- the V_{CC} undervoltage lockout ($V_{disable2}$) level is increased from 9 V up to 12.5 V. This limitation of the V_{CC} hysteresis enables to increase the pulsed mode frequency
- the peak inductor current is forced to be constant and equal to the level programmable by the external resistor R_{Ipmax} connected to the pin 9 so that:

$$I_{pmax} = \frac{0,4 \times I_{ref} \times R_{Ipmax}}{2,6 \times R_S}$$

where: I_{pmax} is the standby inductor peak current, R_S is the current sense resistor.

- when the pin 15 current gets higher than the threshold I_{reg} (20.5 × I_{ref}), this operating mode stops and the circuit output is latched off.

So, in fact, the active phase is split into two distinct sequences and finally three phases can be defined (refer to Figure 32):

- the **off phase**: the MC44604 is off and the V_{CC} capacitor is being charged. When the V_{CC} gets higher than $V_{stup-th}$, the circuit turns on and the switching sequence starts
- the **switching phase**: the circuit is on and forces a constant peak inductor current. This sequence lasts until I_{pin15} gets higher than I_{reg}
- the **latched phase**: the circuit is on but the output is disabled. This sequence lasts until the standby V_{CC} undervoltage lockout voltage (12.5 V) is reached. A new off phase is then initialized.

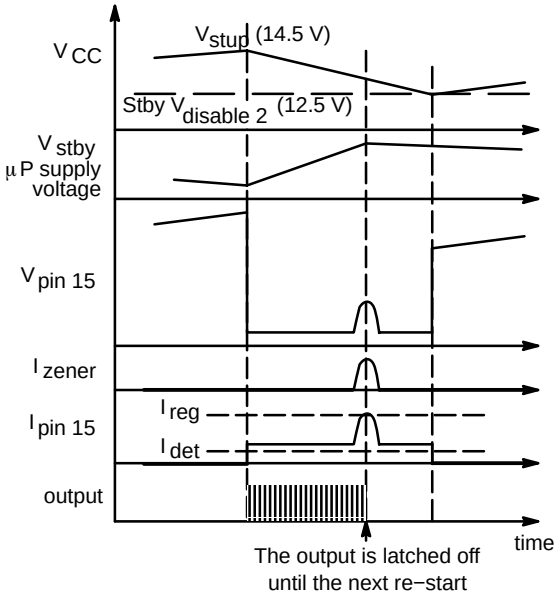


Figure 42. Standby Regulation

As a consequence, V_{stby} varies between a peak value (obtained at the end of the switching phase) and a valley level (reached at the end of the off phase).

The level of the peak value is controlled by forcing a current higher than I_{reg} in pin 15 when this level has reached the desired value.

The arrangement in Figure 41 allows to obtain this operation. A zener diode Z is connected so that a current limited by R_{reg}, is drawn by this device, when the µP supply voltage gets higher than V_z. By this way, the current injected in the pin 15 increases and when this current is detected as higher than I_{reg}, the output gets disabled until the next start−up (Note 1).

Practically, the pin 15 current can be expressed as follows (when the zener is activated):

$$I_{pin15} = CTR \times \frac{V_{stby} - V_{opto} - V_z}{R_{reg}}$$

where: CTR is the opto coupler gain, V_{opto} is opto coupler voltage drop.

So, as the Vstby peak value is obtained when ($I_{pin15} = I_{reg}$), it can be calculated using the following equation:

$$V_{stby\,pk} = V_z + V_{opto} + \frac{R_{reg} \times I_{reg}}{CTR}$$

Practically, R_{reg} is chosen very low (in the range of 10 Ω, low resistance just to limit the current when $V_{stby\,pk}$ gets higher than V_z):

$$V_{stby\,pk} \cong V_z + V_{opto}$$

Note 1. If the pin 15 current is higher than I_{reg} at start−up, the output is just shutdown but not latched. The circuit must detect a sequence during which I_{pin15} lower than I_{reg} before being able to latch gets higher than V_z).

Transitions Between Normal Mode and Standby Mode (Refer to Figure 43)

The MC44604 detects a transition by comparing the pin 15 current to:

- I_{det} (transition standby to normal mode)
- I_{init} (transition normal mode to standby)

Each transition detection results in the circuit turning off, so that the device can work in the new mode after the following restart.

• transition normal mode to standby:

This transition is detected by comparing the I_{pin15} current to the threshold current (I_{init}).

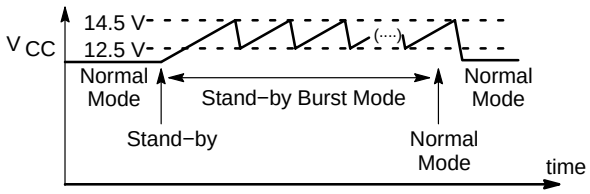
I_{init} is high enough so that the opto coupler current used for the regulation, never exceeds this value.

The arrangement in Figure 41 is well adapted to this mode of operation. The µP initializes the standby mode by turning on the switch T. This results in the C capacitor charge that produces a peak current in the primary side of the opto coupler. C and R_{init} must be dimensioned so that the opto coupler primary side generates a pin 15 current higher than I_{init} during more than 1 µs.

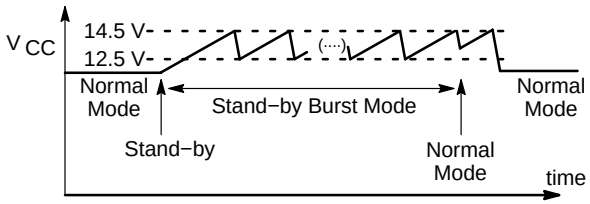
• transition standby to normal mode:

If the circuit detects that ($I_{pin15} < I_{det}$) during standby operation, the circuit is turned off. So, if the normal mode is maintained at the following start−up, the circuit will re−start in a normal mode configuration.

The arrangement in Figure 41 allows to perform this detection. When the µP detects the end of the standby, it turns off the switch T and the opto coupler stops supplying current to the circuit.



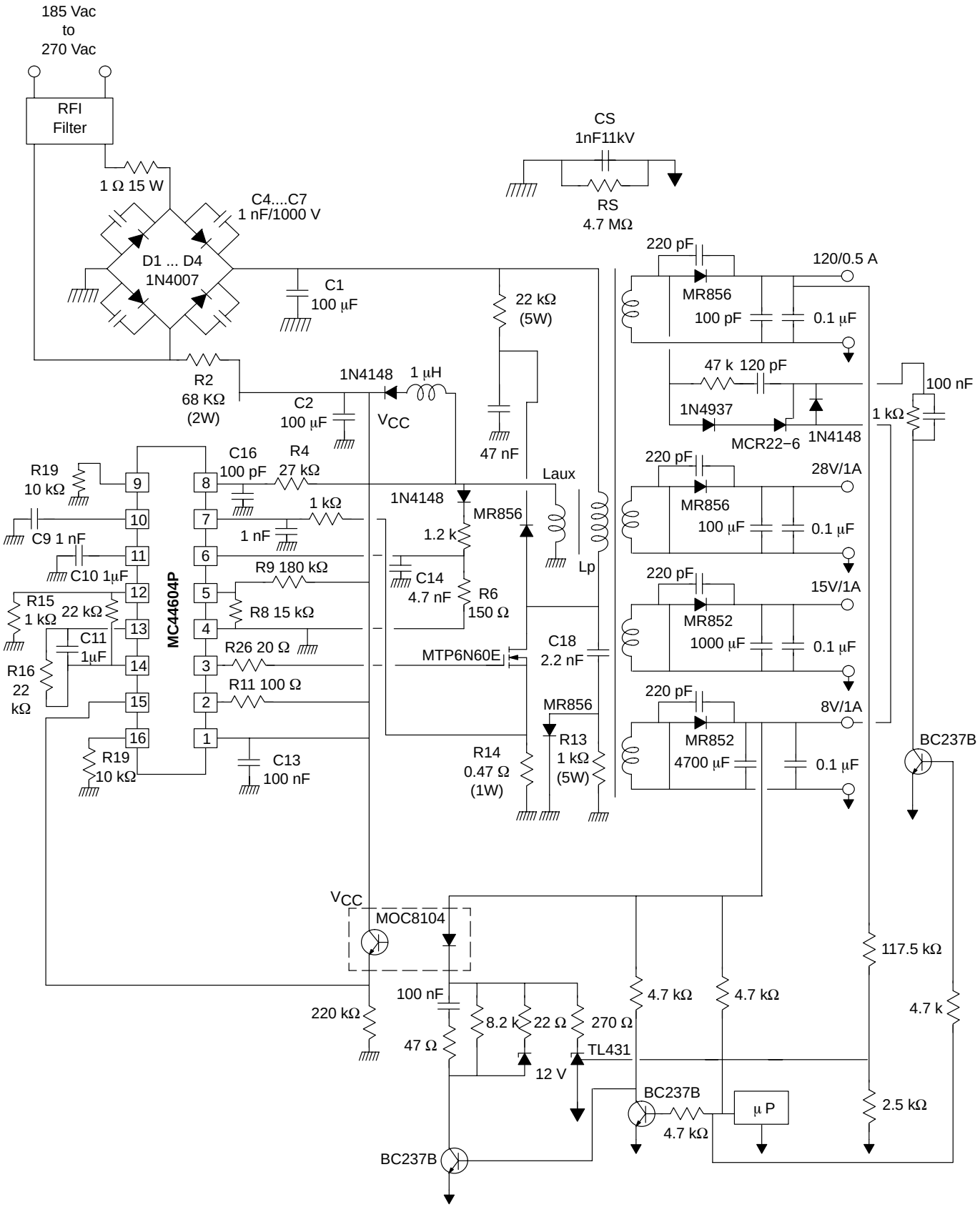
The transition stand−by to normal mode occurs while the circuit is off (V_{CC} charge phase)



The transition stand−by to normal mode occurs while the circuit is on (working phase)

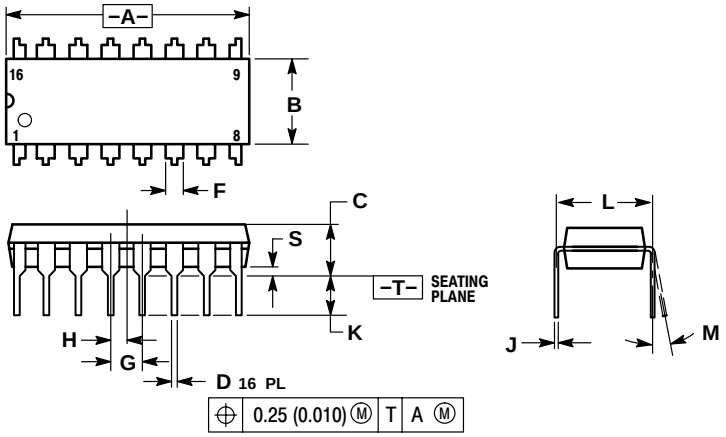
Figure 43. Transitions Between Modes

Application Schematic



PACKAGE DIMENSIONS

PDIP−16
P SUFFIX
CASE 648−08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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