NS4205 User Manual V1.1

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Revision history

dates	releases	author	Modification Instructions

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1 Functional Description

The NS4205 is a filter-less, Class D binaural audio amplifier that employs advanced technology to dramatically reduce EMI interference over the full bandwidth range, minimizing the impact on other components.The filter-less PWM modulation structure and built-in feedback resistors of the NS4205 reduces external components, PCB area, and system cost. The NS4205 has built-in over-current protection, over-temperature protection and under-voltage protection, which effectively protects the chip from being damaged under abnormal operating conditions. In addition, the new circuit design is fully optimized by spread spectrum technology, and the efficiency of up to 90% is more suitable for portable audio products.

The NS4205 is available in a SOP16 package and is rated for operation over the -40°C to 85°C temperature range.

2 Main characteristics

- 3W Output Power (Vdd=5.0V,RL=4Ω)
- 0.2% THD (0.5W output power, 5V supply)
- Excellent full bandwidth EMI suppression
- 90% efficiency
- High PSRR: -80dB (217Hz)
- Operating voltage range: 3.0V to 5.25V
- Over-current protection, overheating protection, under-voltage protection
- SOP16 package

3 Application Areas

- Low voltage sound system

4 Typical Application Circuit

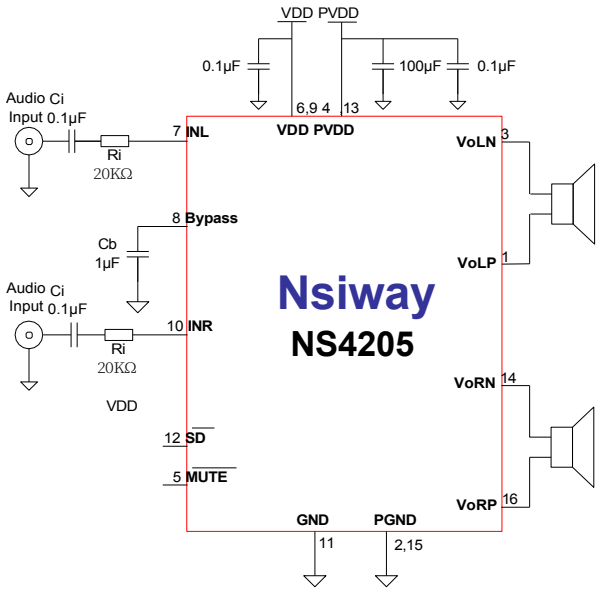


Figure 1 Typical NS4205 Application Circuit

5 limit parameter

Table 1 Maximum physical limits of the chip

parameters	minimum value	maximum values	unit (of measure)	clarification
Supply Voltage	2.8	5.5	V	
Storage temperature	-65	150	oC	
Input Voltage	-0.3	VDD	V	
ESD Voltage Resistance	4000		V	
temperature of a bond	150		oC	
operating temperature	-40	85	oC	
thermal resistance				
θ_{JC} (SOP16)		20	°C/W	
θ_{JA} (SOP16)		80	°C/W	
welding temperature		220	oC	Within 15 seconds

Note: The operating performance of the chip is not guaranteed outside the limits or under any other conditions.

6 Electrical Characteristics

Limiting conditions: (T_A = 25°C)

Table 2 NS4205 Electrical Characteristics

notation	parameters	test condition	minimum value	standard value	maximum values	unit (of measure)
VDD	Supply Voltage		3.0		5.25	V
IDD	Power supply quiescent current	V_{DD} = 3.6V. V_{IN} = 0V, No load		10		mA
		V_{DD} = 5.0V. V_{IN} = 0V, No load		12		mA
IMUTE	Standby Current	V_{DD} = 3.6V, V_{IN} = 0V $V_{/MUTE}$ =0V, No load		8		mA
		V_{DD} = 5.0V, V_{IN} = 0V $V_{/MUTE}$ =0V, No load		10		mA
ISD	Off Leakage Current	$V_{/SD}$ =0V		1	20	μA
VOS	Output Offset Voltage			10	40	mV
R_O	output resistance			3		KΩ
PSRR	Power Supply Rejection Ratio	217Hz			-80	dB
		20KHz			-72	dB
CMRR	Common mode rejection ratio			-70		dB
fSW	modulation frequency	V_{DD} =3V to 5.25V		450		kHz
η	efficiency	Po=1.5W. R_L =4Ω,V_{DD} =3.6V		90		%
	logical console					

		THD = 10%, f=1KHz,R_L =4Ω		3.0		W
		THD=1%, f=1KHz,R_L =8Ω		1.3		W
		THD=10%, f=1KHz,R_L =8Ω		1.8		W
THD+N	Total Distortion + Noise	20Hz≤f≤20KHz R_L = 4Ω/8Ω, P_O = 0.5W		0.2		%
Stereo Isolation	stereo separation	RL=4Ω,Po=0.5W		-80		dB
SNR	signal-to-noise ratio	RL=4Ω,Po=1.5W		80		dB

7 Chip Pin Description

7.1 Pin Assignment Diagram

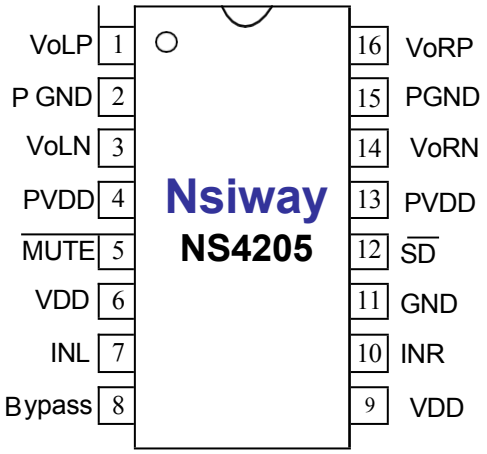


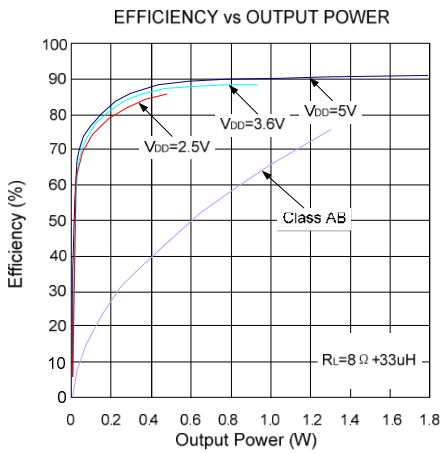
Figure 2 Pin Assignment Diagram for SOP16 Package (top view)

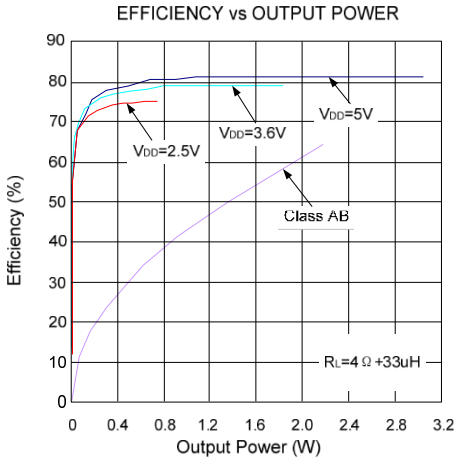
7.2 Pin Function Description

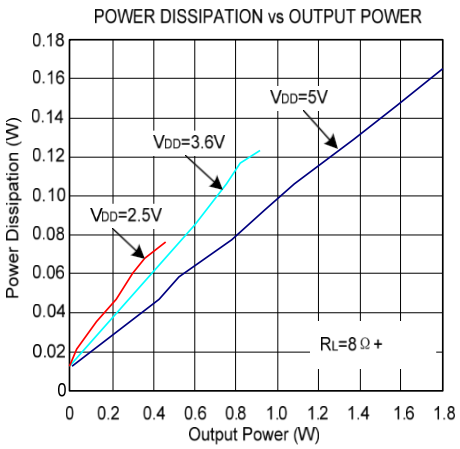
Table 3 NS4205 Pin Descriptions

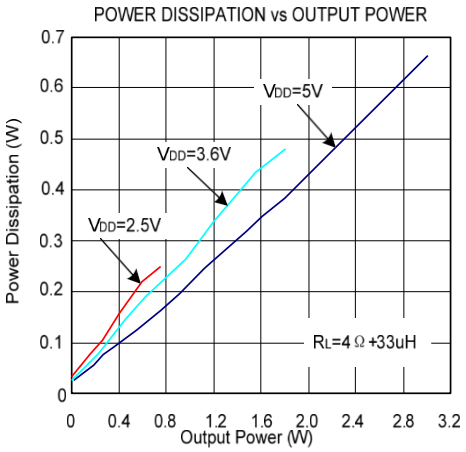
notation	pin number	descriptive
VoLP	1	Positive left channel output
PGND	2	powerfully
VoLN	3	Left channel output negative
PVDD	4	Power Supply Input
/MUTE	5	Standby control, active low (standby)
VDD	6	Power Input
INL	7	Left channel input
Bypass	8	bypass capacitor
VDD	9	Power Input
INR	10	Right channel input
GND	11	POWER GROUND
/SD	12	Shutdown control, active low (shutdown)
PVDD	13	Power Supply Input
VoRN	14	Negative right channel output
PGND	15	powerfully
VoRP	16	Positive right channel output

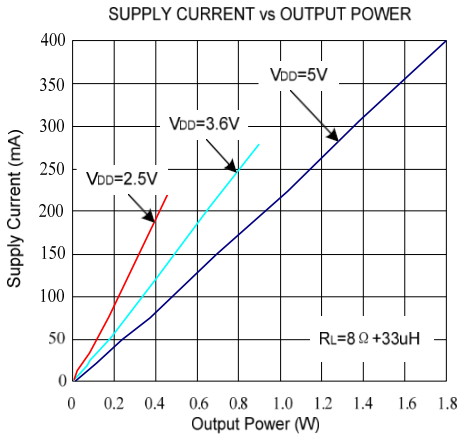
8 NS4205 Typical Reference Characteristics

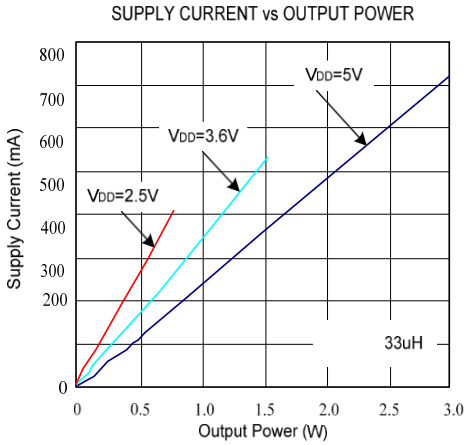


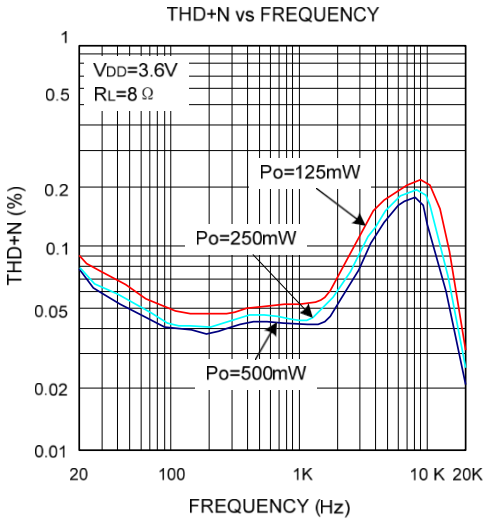


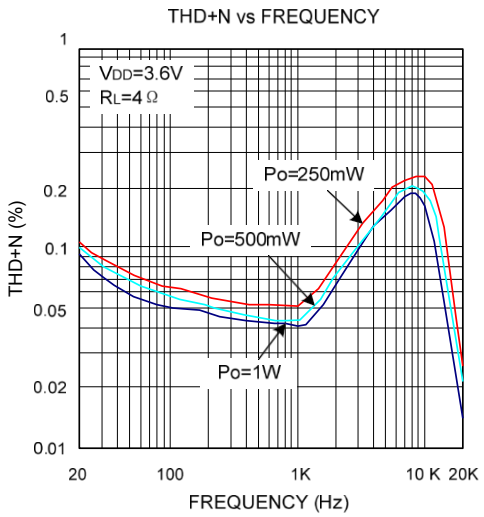

POWER DISSIPATION vs OUTPUT POWER
Power Dissipation (W)
Output Power (W)
VDD=5V
VDD=3.6V
VDD=2.5V
RL=8Ω+


POWER DISSIPATION vs OUTPUT POWER
Power Dissipation (W)
Output Power (W)
VDD=5V
VDD=3.6V
VDD=2.5V
RL=4Ω+33uH

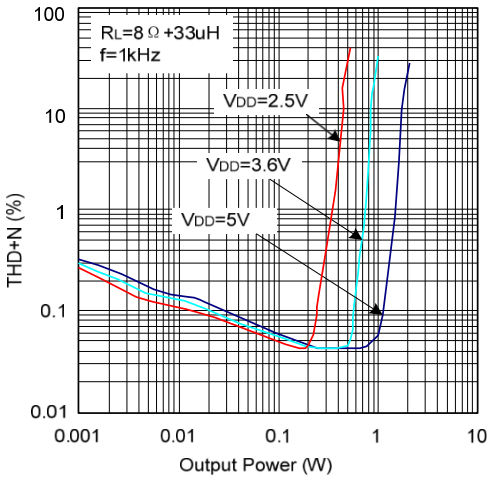

SUPPLY CURRENT vs OUTPUT POWER
Supply Current (mA)
Output Power (W)
VDD=5V
VDD=3.6V
VDD=2.5V
RL=8Ω+33uH


SUPPLY CURRENT vs OUTPUT POWER
Supply Current (mA)
Output Power (W)
VDD=5V
VDD=3.6V
VDD=2.5V
33uH

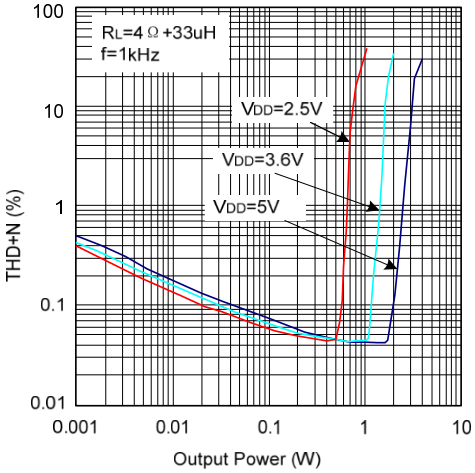

THD+N vs FREQUENCY
THD+N (%)
FREQUENCY (Hz)
VDD=3.6V
RL=8Ω
Po=125mW
Po=250mW
Po=500mW


THD+N vs FREQUENCY
THD+N (%)
FREQUENCY (Hz)
VDD=3.6V
RL=4Ω
Po=250mW
Po=500mW
Po=1W

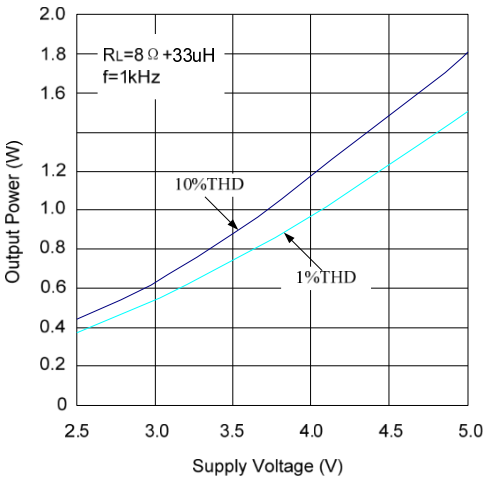
THD+N vs OUTPUT POWER



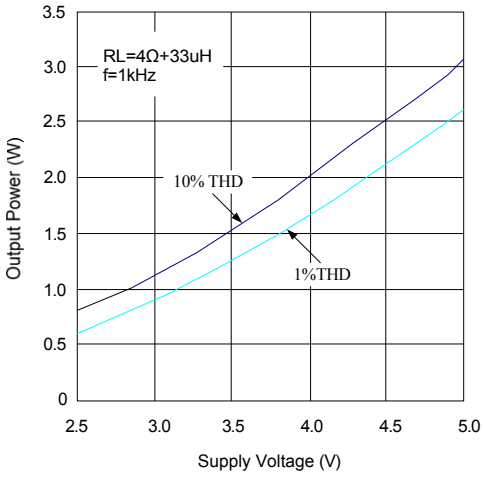
THD+N vs OUTPUT POWER



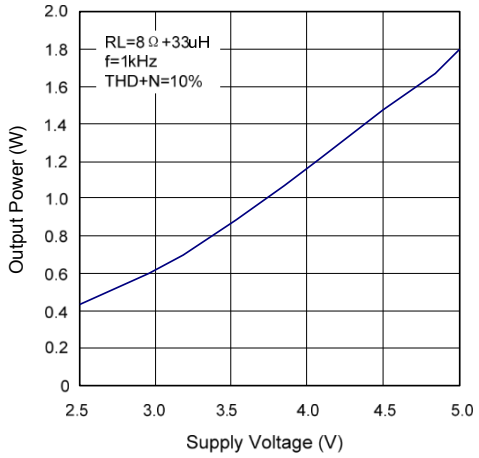
OUTPUT POWER vs SUPPLY VOLTAGE



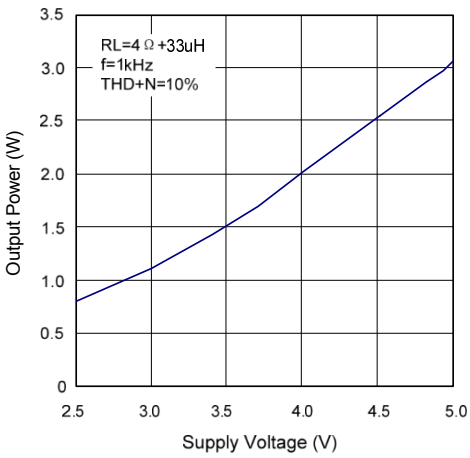
OUTPUT POWER vs SUPPLY VOLTAGE



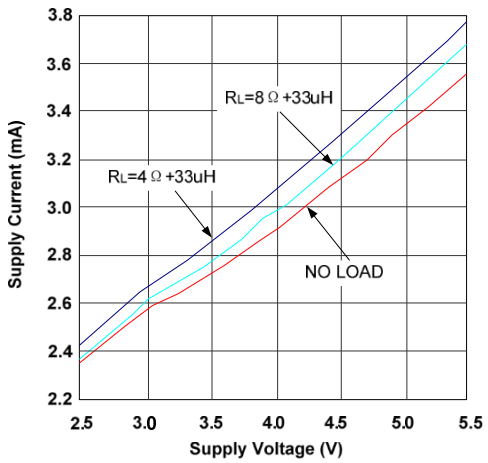
OUTPUT POWER vs SUPPLY VOLTAGE



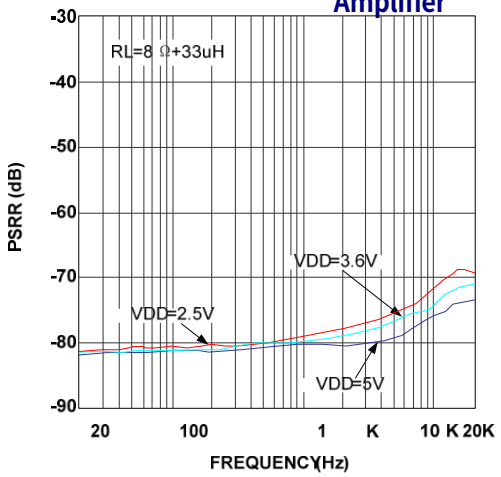
OUTPUT POWER vs SUPPLY VOLTAGE



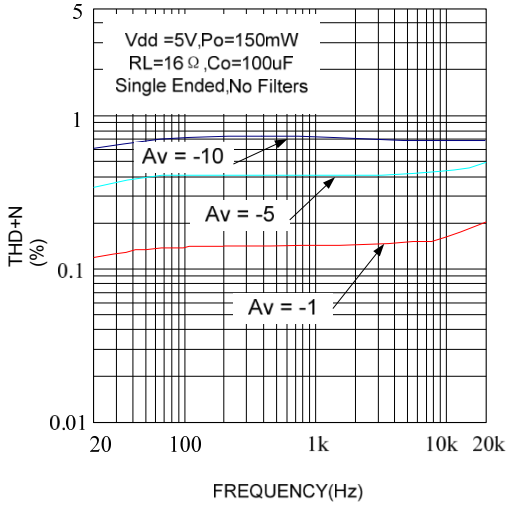
SUPPLY CURRENT vs SUPPLY VOLTAGE



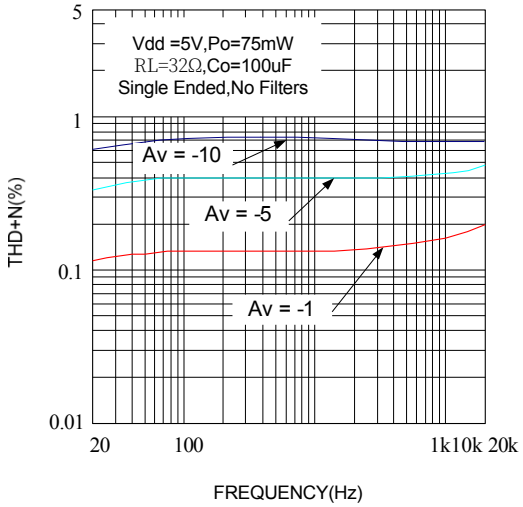
PSRR vs FREQUENCY



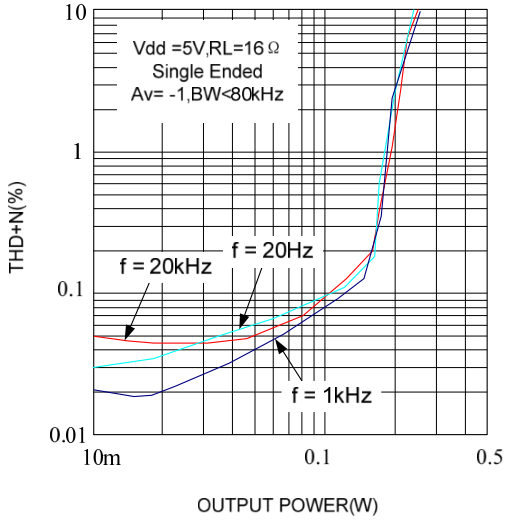
THD+N vs Frequency



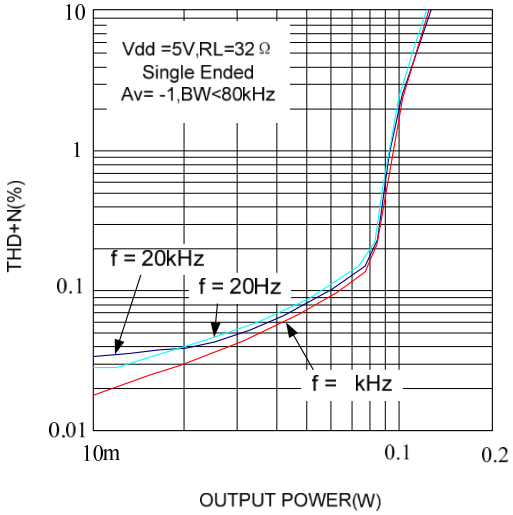
THD+N vs Frequency

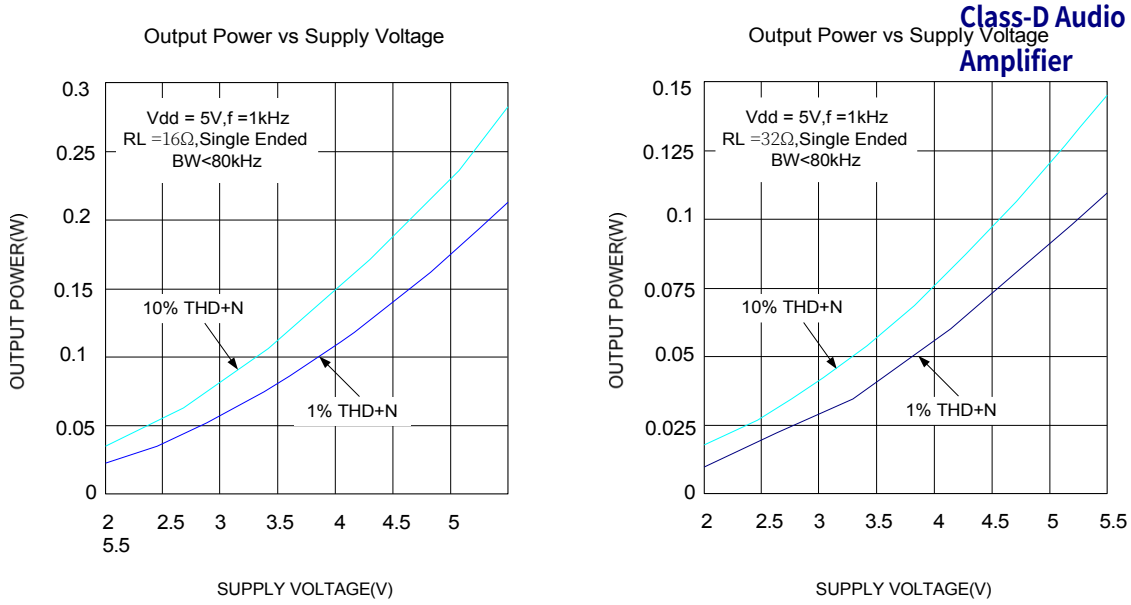


THD+N vs Output Power



THD+N vs Output Power





9 NS4205 Application Notes

9.1 Description of the basic structure of the chip

The NS4205 is a filter-less, Class D, two-channel audio amplifier. The NS4205 is a filter-less, Class D bi-channel audio amplifier with integrated feedback resistors for each channel. The gain of the amplifier can be set peripherally by the input resistors, and the BTL outputs. The block diagram is shown below:

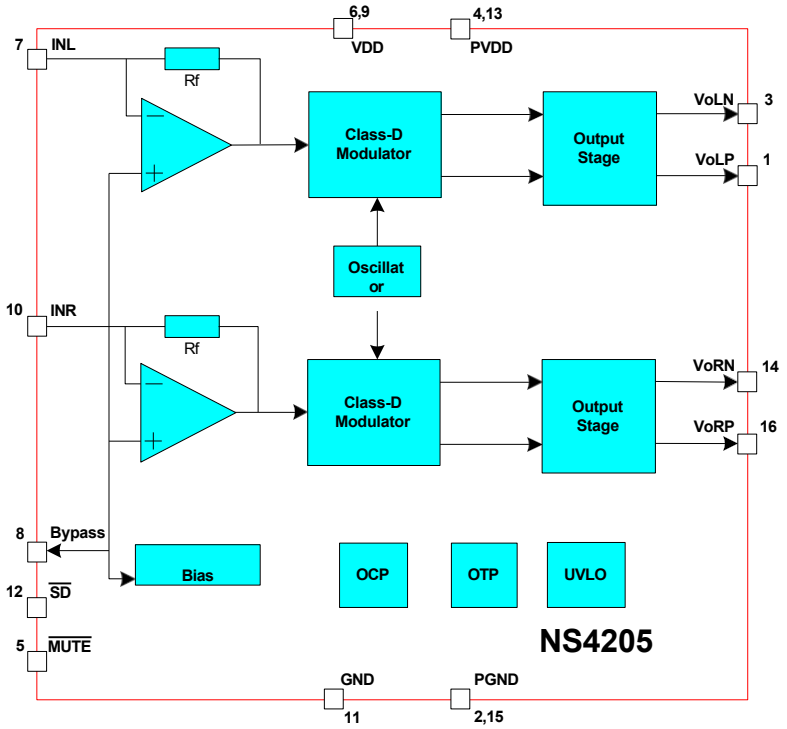


Figure 3 NS4205 Block Diagram

9.2 NS4205 Operating Modes

The operating modes of the NS4205 are set via pins /SD and /MUTE as follows

Table 4 NS4205 Operating Mode Settings

/SD	/MUTE	operating mode
your (honorific)	your (honorific)	Normal Operating Mode
your (honorific)	lower (one's head)	standby mode
lower (one's head)	Low/High	Low power shutdown

Bridge Output Mode

The gain of the internal modulation stage is 3. The total gain per channel is Av= 240K/Ri.

Input Capacitance Ci and Input Resistance Ri Selection

The input capacitor and input resistor form a high-pass filter with a cutoff frequency of $f_{-3dB} = \frac{1}{2\pi R_{IN} C_I}$. Excessive input capacitance increases into cost and increase area, which is very unfavorable for cost and area constrained applications. Obviously, it is important to determine how much capacitance to use to accomplish coupling. In fact, in many applications, speakers are not capable of reproducing low frequency speech below 100Hz-150Hz, so using large capacitance does not improve system performance. In addition to system performance considerations, the suppression of switching/toggle noise is affected by the capacitance. If the coupling capacitance is large, the delay in the feedback network is large, resulting in pop noise, which can therefore be reduced by a small coupling capacitance.

Bypass Capacitance Cb Selection

Cb determines the stability of the NS4205's static operating point, so its value is critical when turning on input signals with bursts. the larger Cb is, the slower the chip's output tilts to the static DC voltage (i.e., VDD/2), and the smaller the bursts will be when turning it on. 1uF of Cb gives a shutdown function that has both less ticking and less bursting. A Cb of 1uF results in a shutdown function with less "ticking" and less "popping".

Power supply filter capacitor selection

In the application of amplifiers, the bypass design of the power supply is important, especially for the noise performance and supply voltage rejection of the application program

The design requires the filter capacitor to be as close as possible to the power supply pin of the chip. The design requires that the filter capacitors be placed as close as possible to the power supply pin of the chip. A typical capacitor is a 100uF electrolytic capacitor with a 0.1uF ceramic capacitor.

Low power shutdown function

When the /SD pin is low, the chip is in a shutdown low-power state. There is an internal pull-up resistor, and the /SD pin can be left open.

Standby state control function

When the /SD pin level is high and the /MUTE pin level is low. The chip enters the standby state. There is an internal pull-up resistor, and the /MUTE pin can be suspended.

9.3 EMI Enhanced Technology

The NS4205 has built-in EMI enhancement technology. Using advanced technology, EMI

interference is greatly reduced over the full bandwidth range, minimizing the impact on other components. This is shown in the figure below.

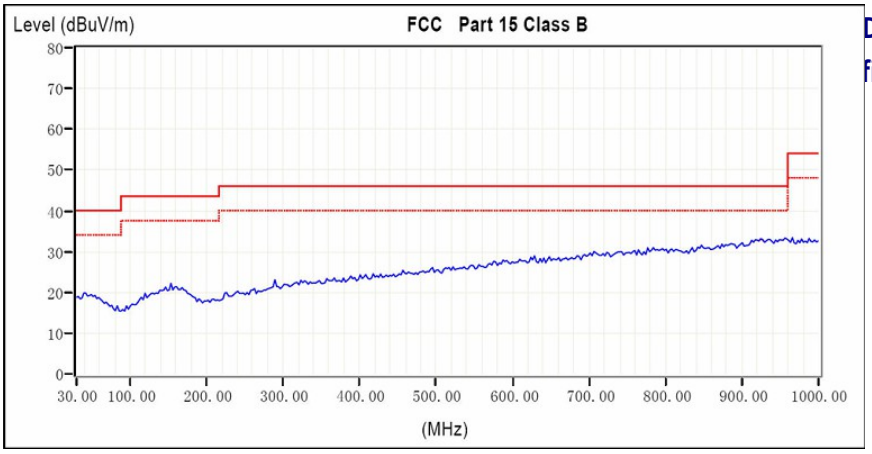


Figure 4 EMI Test Spectrum

9.4 effi cien cy

The NS4205 utilizes extended spectrum technology to fully optimize the circuit design of the new Class D amplifier for improved efficiency. Efficiencies of up to 90% are ideal for portable audio products.

9.5 protection circuit

When the chip experiences a short circuit between an output pin and power or ground, or a short circuit fault between outputs, the overcurrent protection circuit shuts down the chip to prevent it from being damaged. After the short circuit fault is removed, the NS4205 automatically resumes operation. The chip is also shut down when the temperature of the chip is too high. After the temperature drops, the NS4205 continues to work normally. When the supply voltage is too low, the chip will also be shut down, and after the supply voltage is restored, the chip will start again.

10 NS4205 Application Notes

1. Amplifier output to the speaker alignment, connecting lines as short as possible, as wide as possible, and output wiring, connecting lines as far away as possible from sensitive signal lines and circuits.
2. The decoupling capacitor of the power supply pin of the amplifier is as close as possible to the chip pin. The power and ground wires should be connected in a star pattern.
3. Beads and capacitors can be added to the outputs. The beads and capacitors should be placed as close to the chip pins as possible. The following is a reference circuit for the NS4205 application design with beads added:

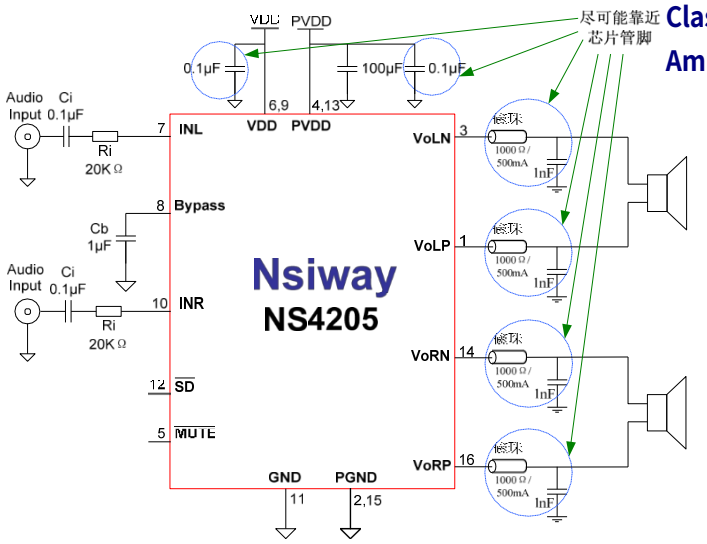
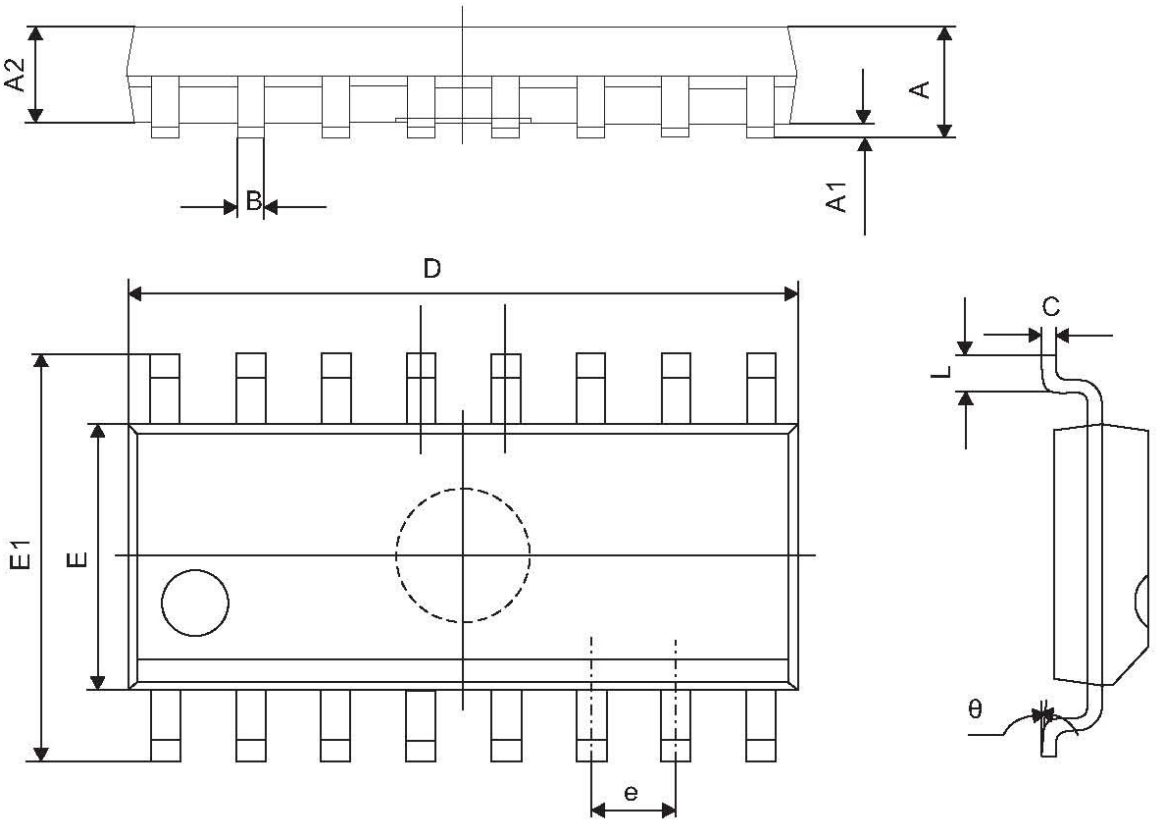


Figure 5 NS4205 with magnetic bead application circuit

11 Chip Packaging

11.1 SOP16 Package Dimensions



Symbol	Dimensions Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

Figure 6 SOP16 Package Dimensions

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