

N-channel 600 V, 0.550 Ω typ., 7.5 A MDmesh II Plus™ low Q_g
Power MOSFETs in D²PAK, DPAK, TO-220 and IPAK packages

Datasheet – production data

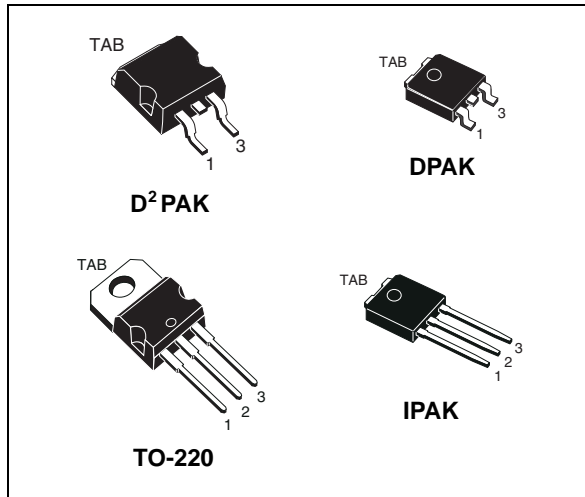
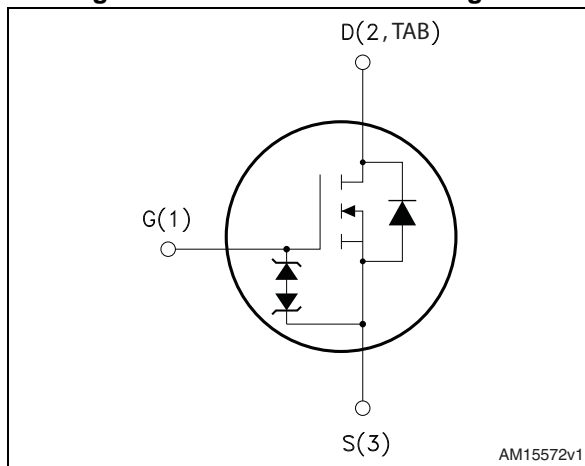


Figure 1. Internal schematic diagram



Features

Order codes	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STB10N60M2	650 V	0.600 Ω	7.5 A
STD10N60M2			
STP10N60M2			
STU10N60M2			

- Extremely low gate charge
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB10N60M2	10N60M2	D ² PAK	Tape and reel
STD10N60M2		DPAK	
STP10N60M2		TO-220	Tube
STU10N60M2		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	30	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	85	W
$dv/dt^{(1)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(2)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. $I_{SD} \leq 7.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD}=400\text{ V}$

2. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	DPAK	TO-220	I ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.47				$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max ⁽¹⁾	30	50			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max			62.5	100	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50$)	110	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		0.550	0.600	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	400	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{riss}	Reverse transfer capacitance		-	0.84	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	83	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 7.5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 17)	-	13.5	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	7.2	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 3.75\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16 and Figure 21)	-	8.8	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	32.5	-	ns
t_f	Fall time		-	13.2	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		30	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7.5 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 18)	-	270		ns
Q_{rr}	Reverse recovery charge		-	2		μC
I_{RRM}	Reverse recovery current		-	14.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 7.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 18)	-	376		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAQ

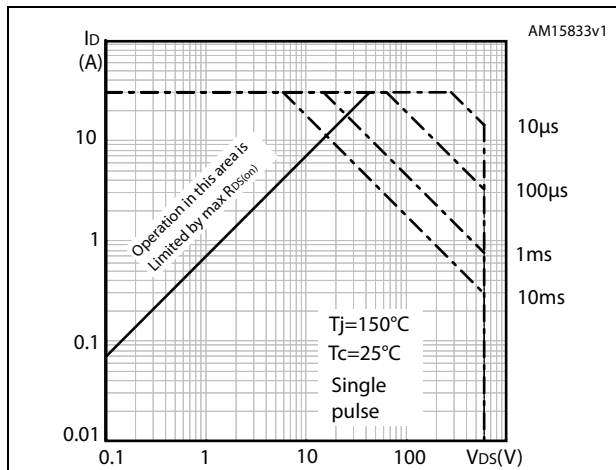


Figure 3. Thermal impedance for DPAK and IPAQ

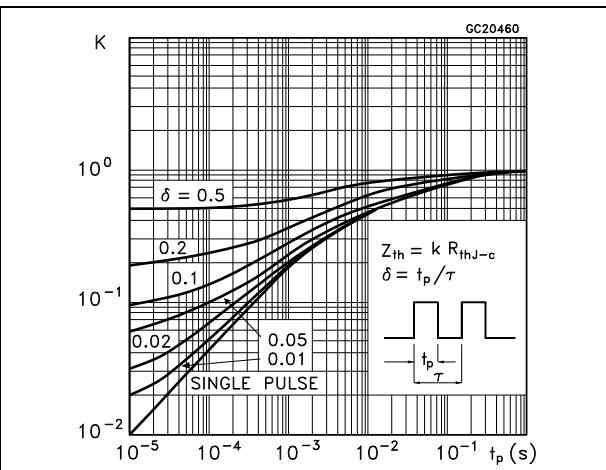


Figure 4. Safe operating area for D²PAK and TO-220

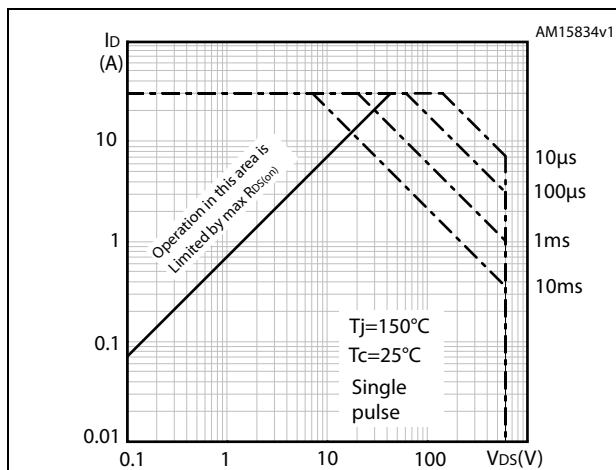


Figure 5. Thermal impedance for D²PAK and TO-220

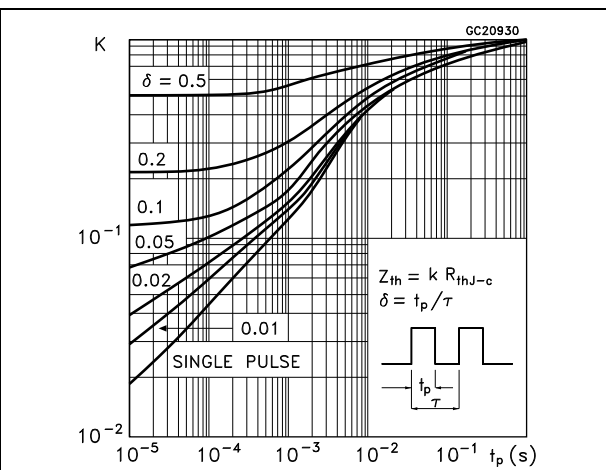


Figure 6. Output characteristics

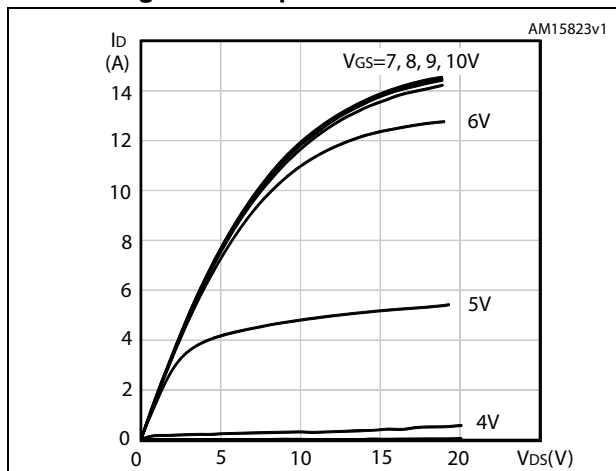


Figure 7. Transfer characteristics

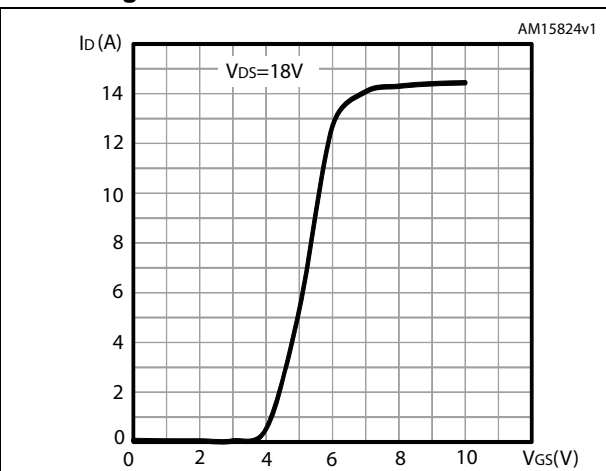


Figure 8. Gate charge vs gate-source voltage

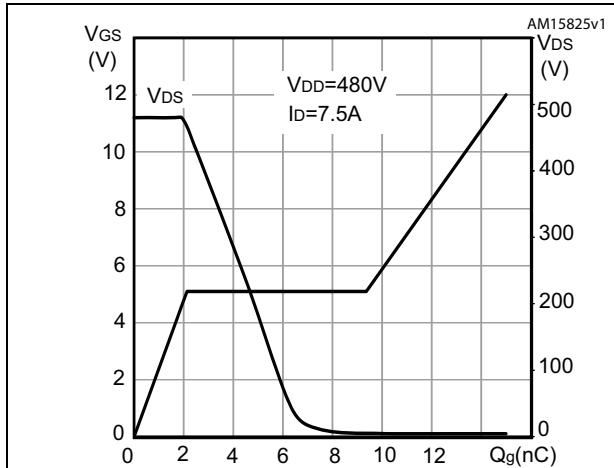


Figure 9. Static drain-source on-resistance

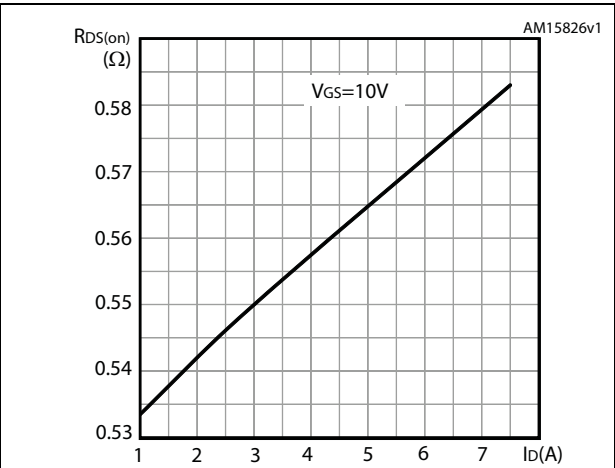


Figure 10. Capacitance variations

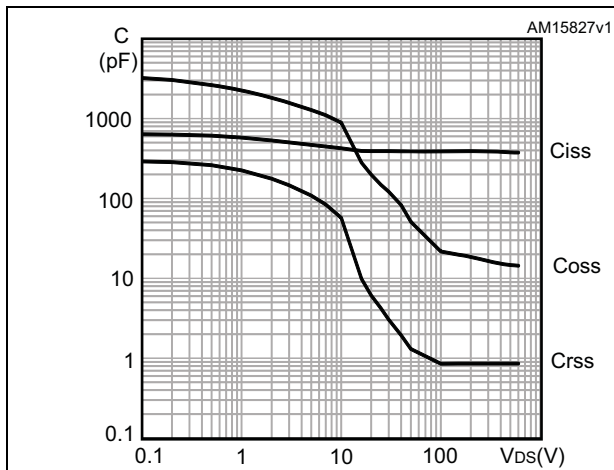


Figure 11. Normalized gate threshold voltage vs. temperature

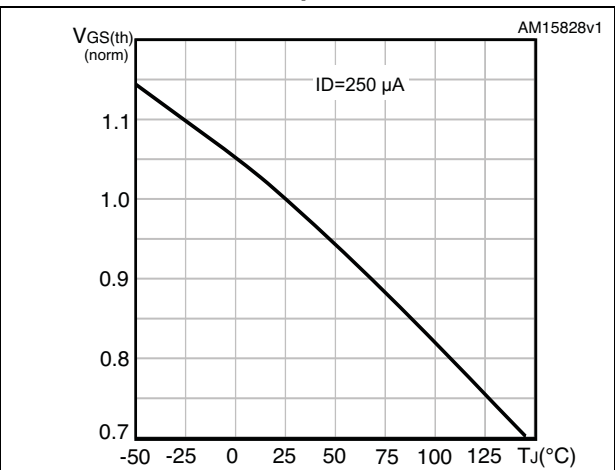


Figure 12. Normalized on-resistance vs temperature

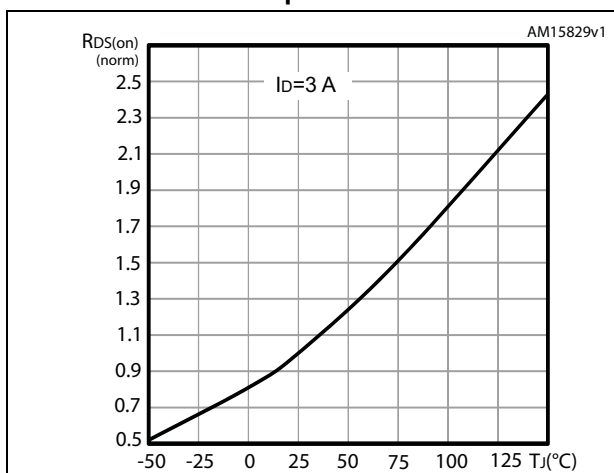


Figure 13. Source-drain diode forward characteristics

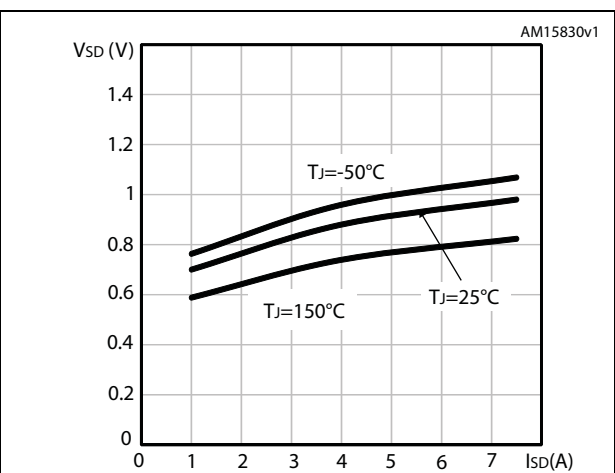


Figure 14. Normalized V_{DS} vs temperature

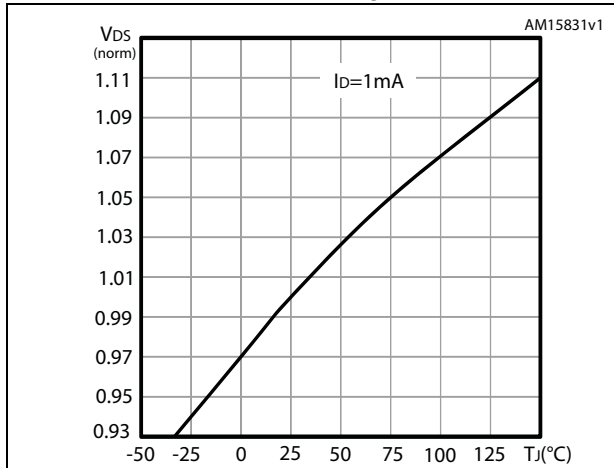
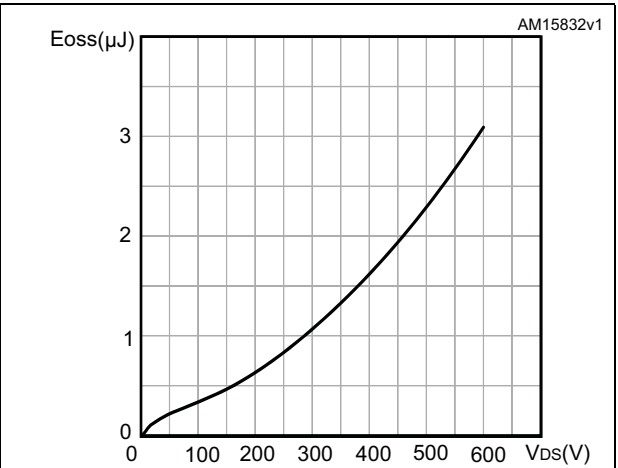
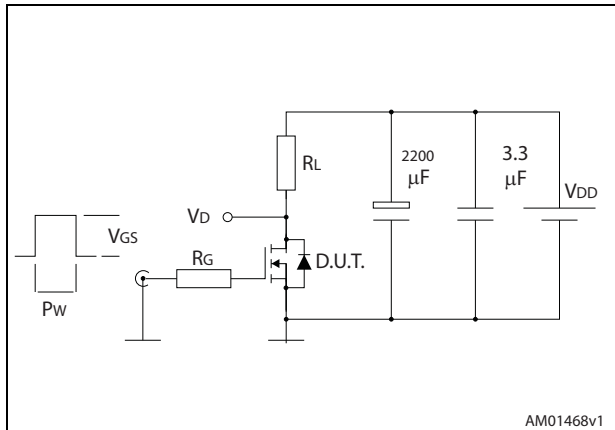


Figure 15. Output capacitance stored energy



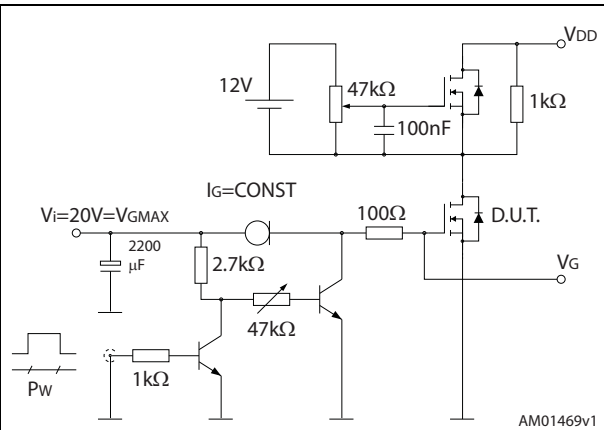
3 Test circuits

Figure 16. Switching times test circuit for resistive load



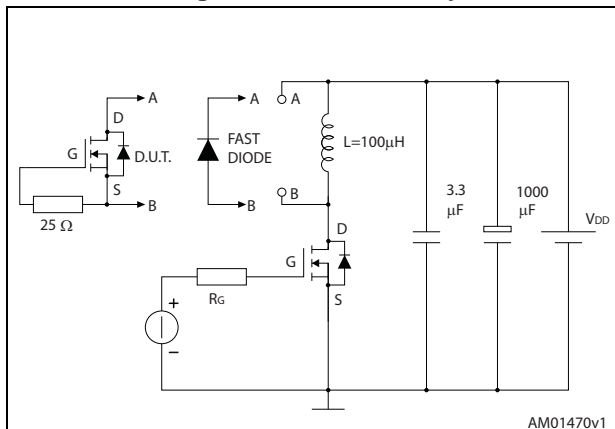
AM01468v1

Figure 17. Gate charge test circuit



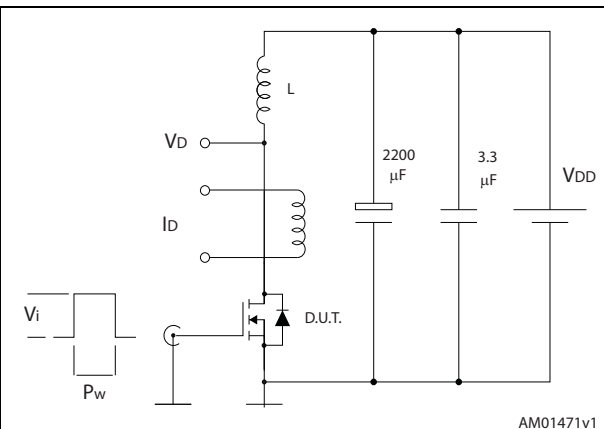
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Figure 18. Test circuit for inductive load switching and diode recovery times



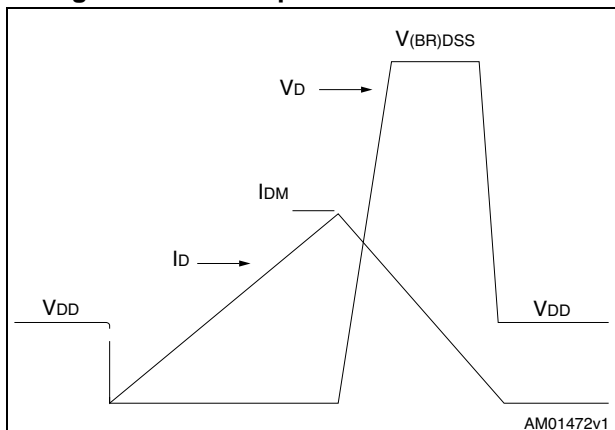
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Figure 19. Unclamped inductive load test circuit



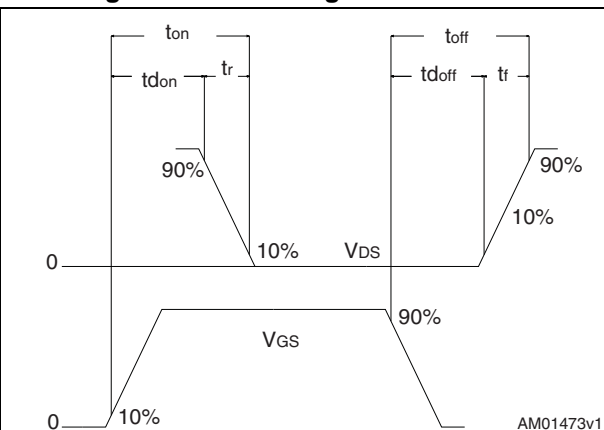
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Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D²PAK (TO-263) drawing

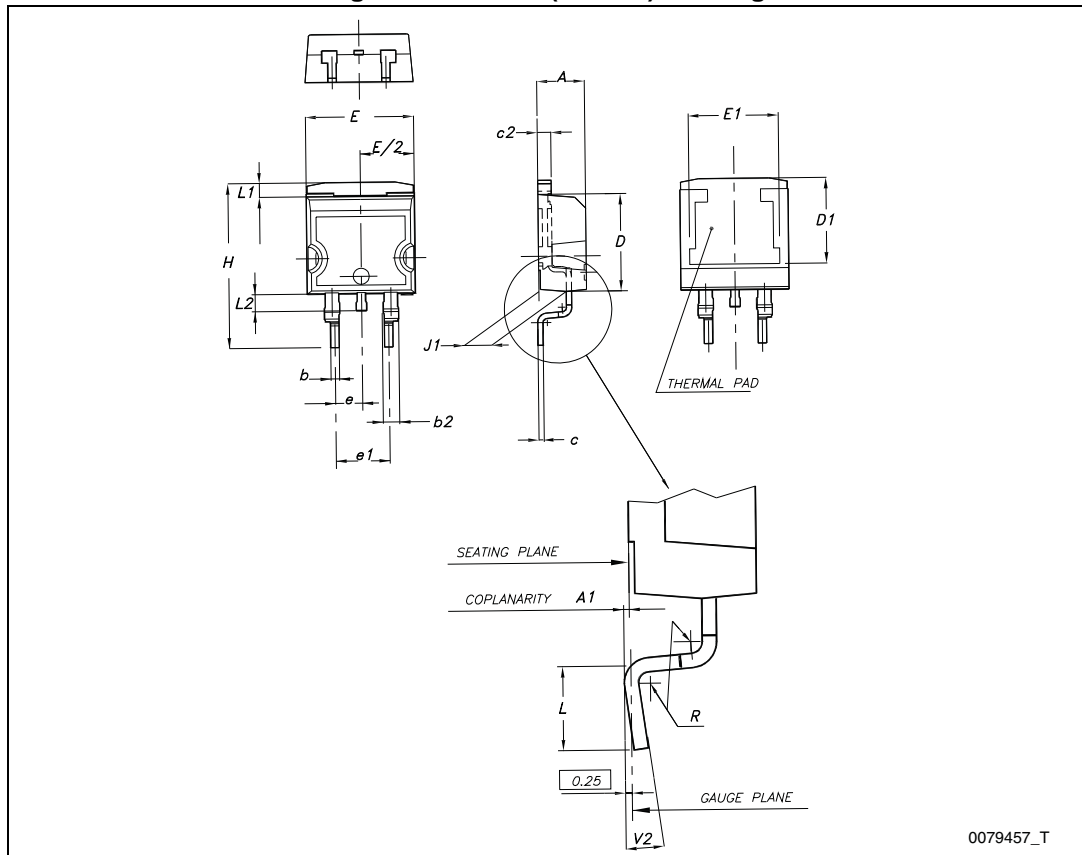
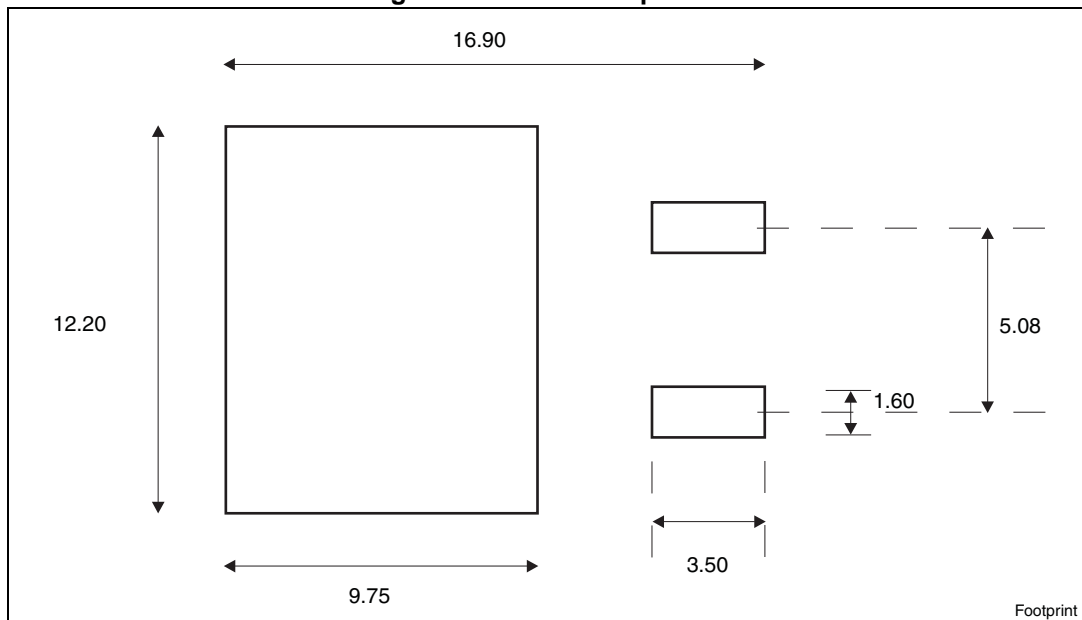


Figure 23. D²PAK footprint^(a)



a. All dimension are in millimeters

Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) type A drawing

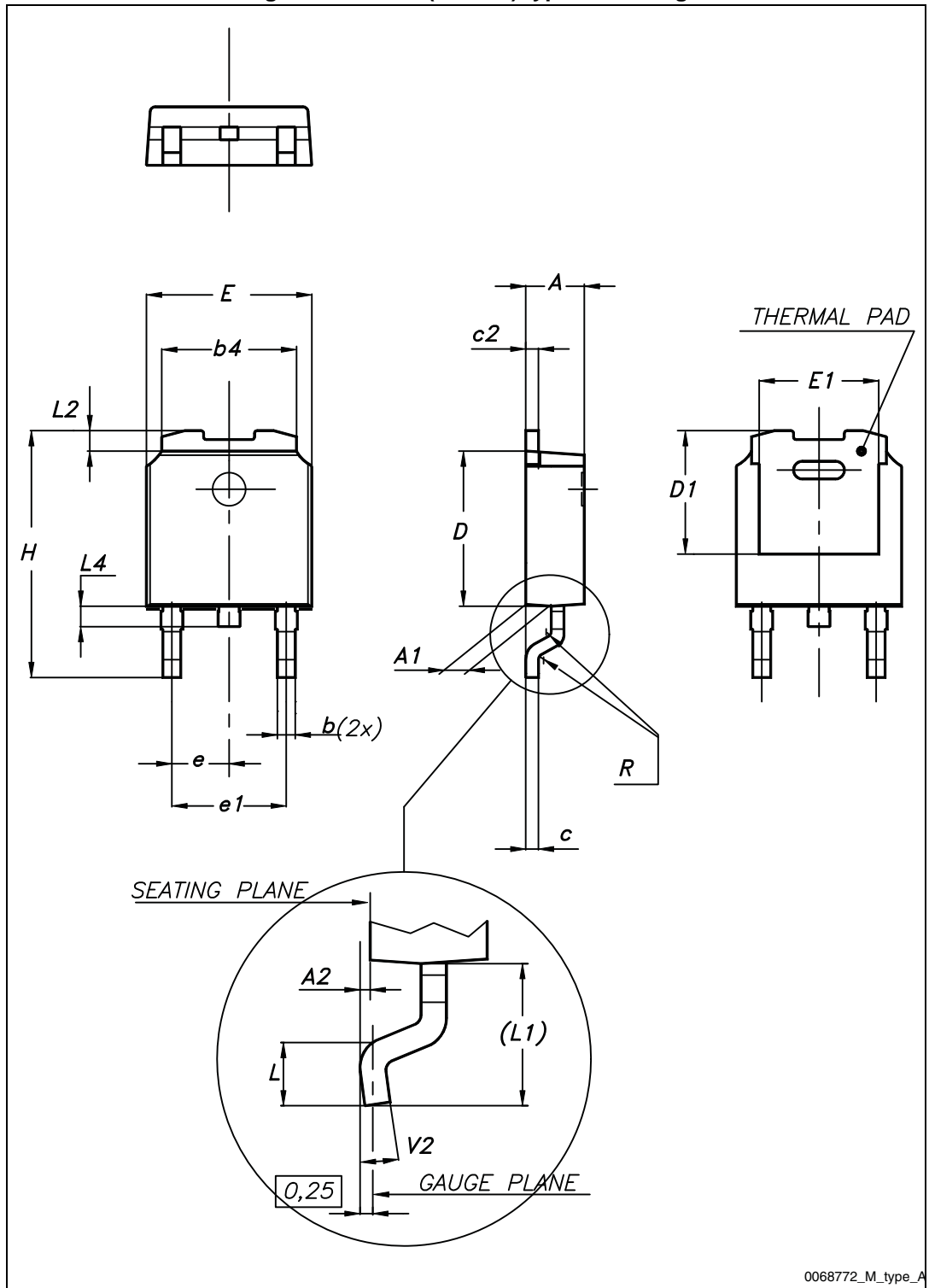
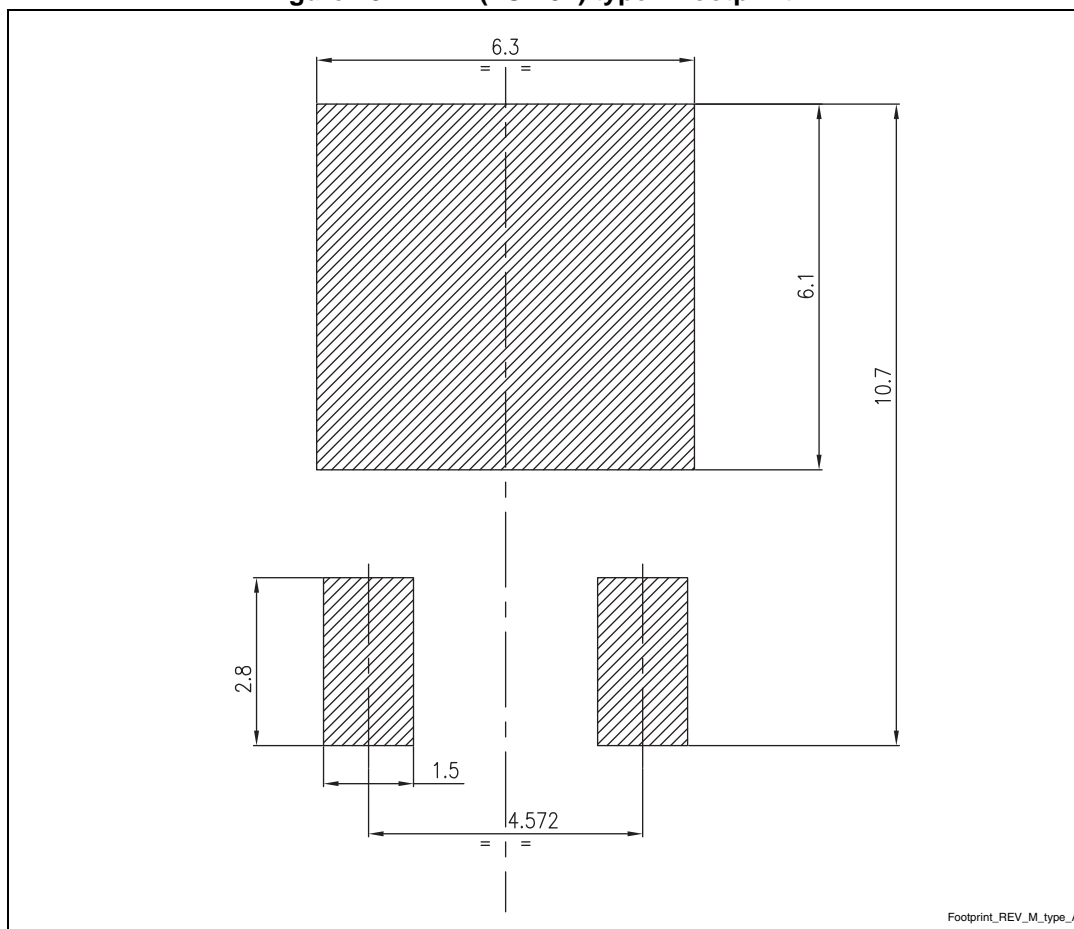


Figure 25. DPAK (TO-252) type A footprint (b)



b. All dimensions are in millimeters

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

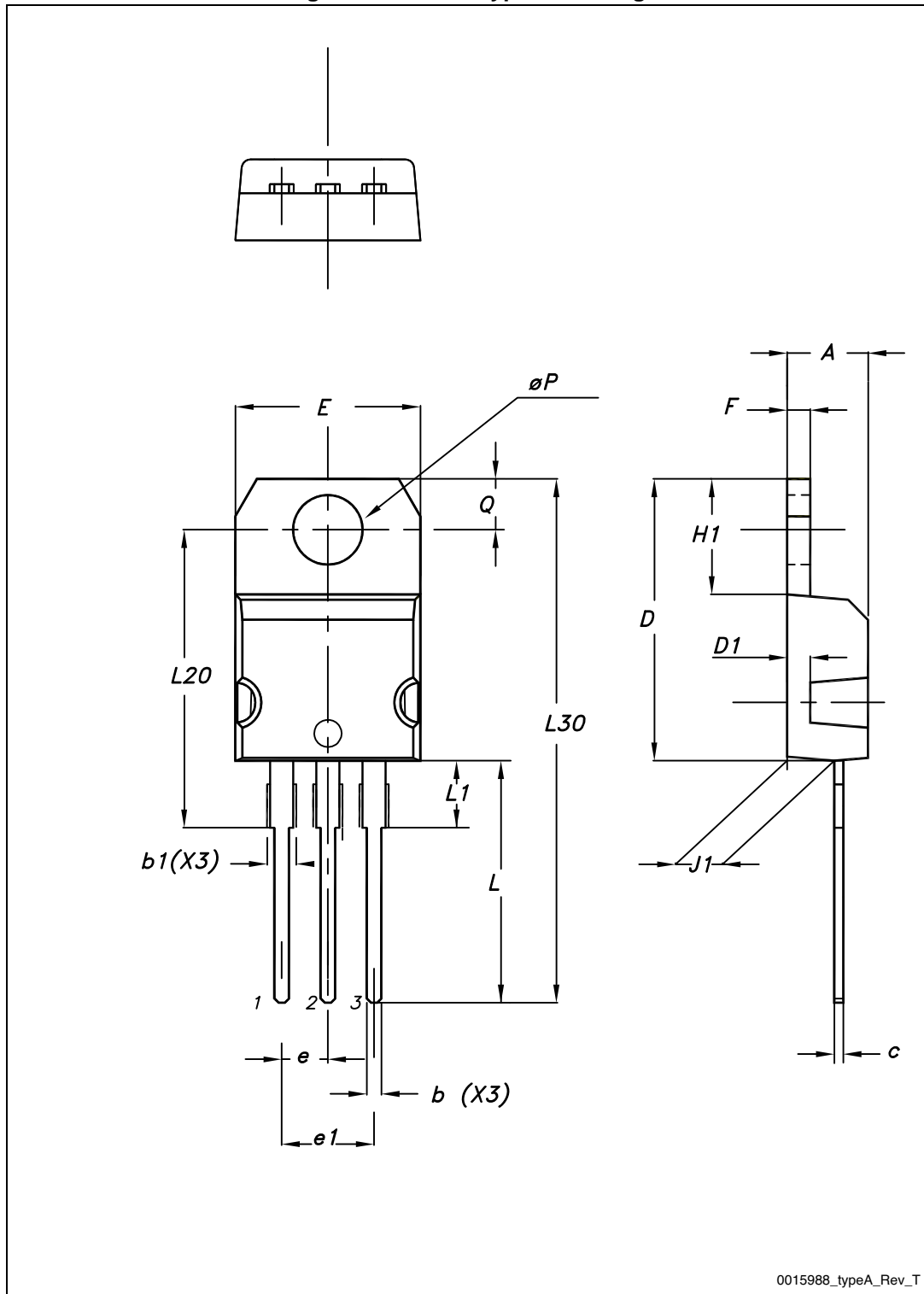
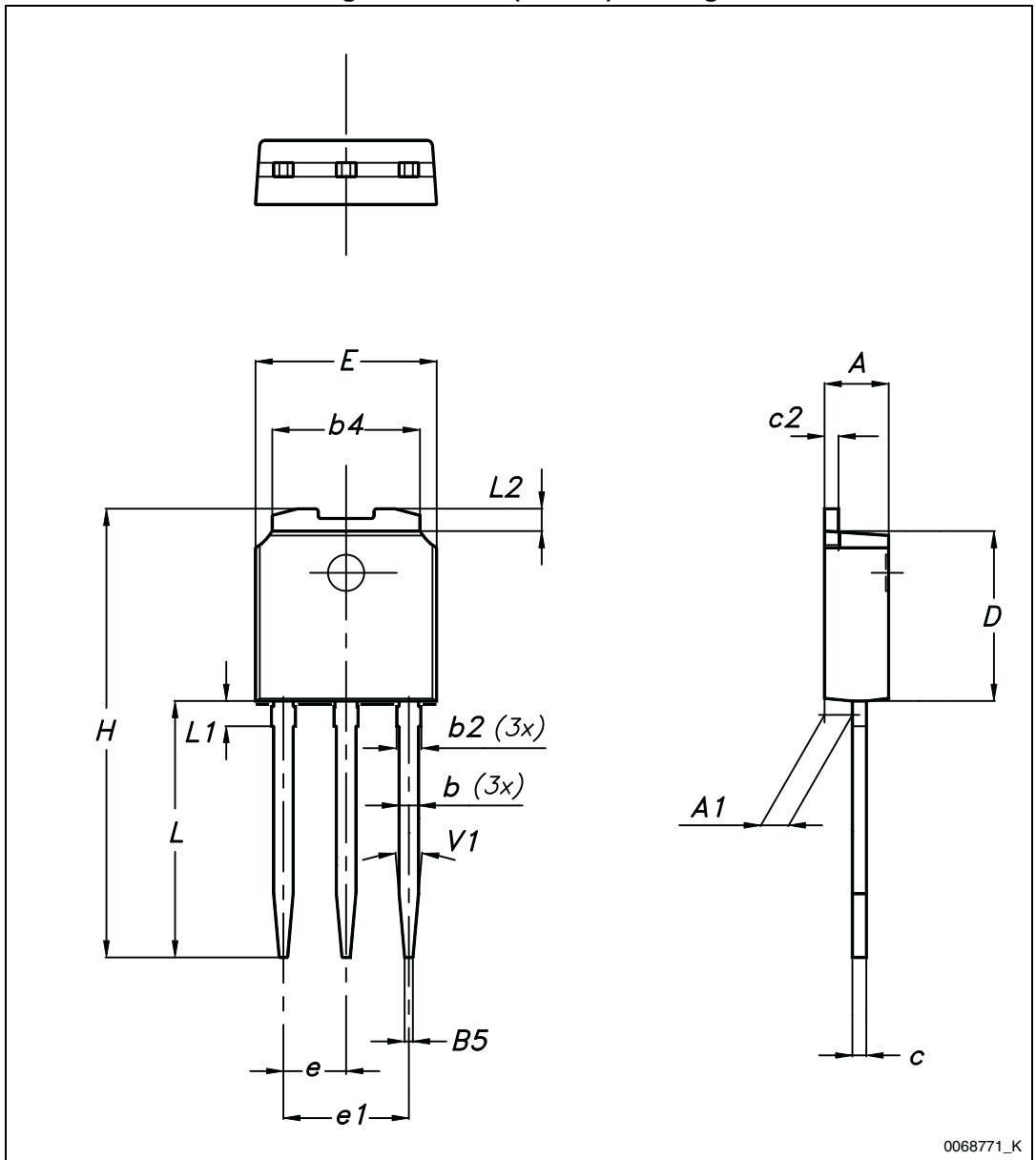


Table 12. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 27. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 28. Tape for D²PAK (TO-263) and DPAK (TO-252)

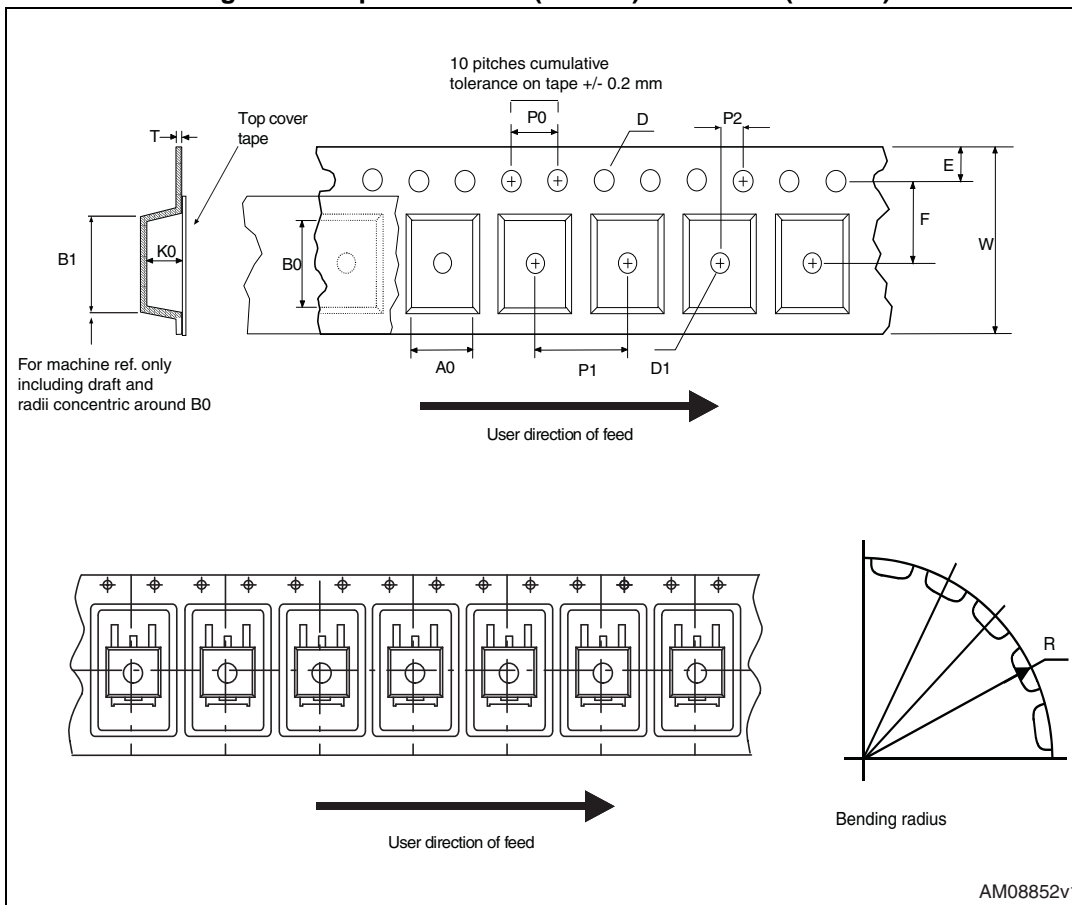
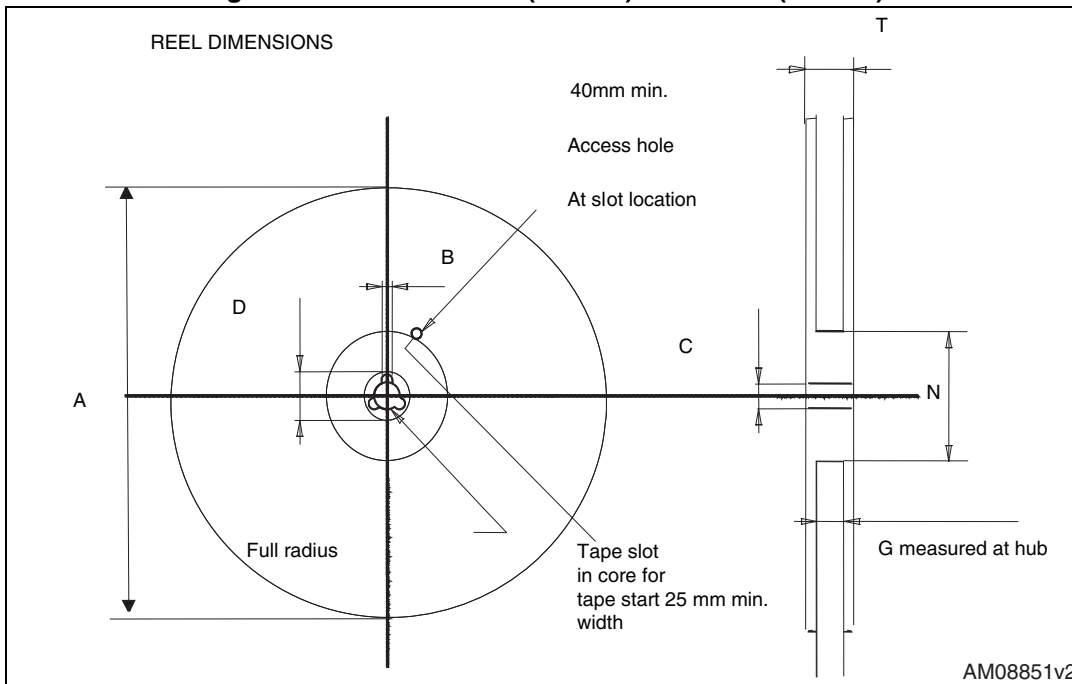


Figure 29. Reel or D²PAK (TO-263) and DPAK (TO-252)



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
29-May-2013	1	First release.
06-Dec-2013	2	<ul style="list-style-type: none">– Added: D²PAK package– Modified: title and $R_{DS(on)}$ values in cover page– Modified: $R_{DS(on)}$ values in Table 5– Modified: R_G value in Table 6– Modified: Figure 9 and I_D value in Figure 12– Added: Table 9, 13, Figure 22 and 23– Updated: Table 10, 11, Figure 24, 25 and 26– Minor text changes

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