TDA2020D

LINEAR INTEGRATED CIRCUIT

40W AUDIO DRIVER

- HIGH SUPPLY VOLTAGE: ± 25V
- HIGH SUPPLY REJECTION: 80 dB
- PROGRAMMABLE SOA PROTECTION
- LOW DISTORTION (0.05% TYP.)
- LOW INPUT NOISE VOLTAGE (4 μV TYP.)

The TDA 2020D is a monolithic integrated **operational amplifier** in a 14 lead quad in-line plastic-package, intended for driving external power transistors in Hi-Fi amplifier (30 to 100W). This device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the external transistors within their safe operating area. A thermal shut-down system is also included. This thermal shut-down can also protect the external power transistors.

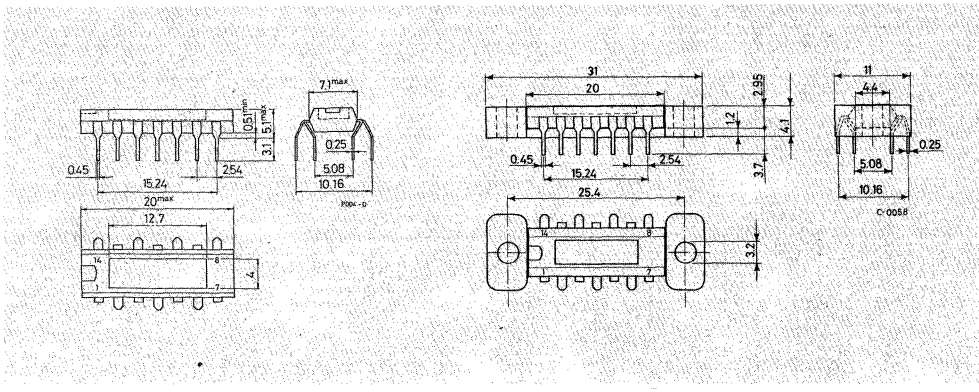
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	± 25	V
V_i	Input voltage	V_s	
V_i	Differential input voltage	± 15	V
I_o	Output peak current	1	A
P_{tot}	Power dissipation at $T_{case} \leqslant 75°C$	25	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

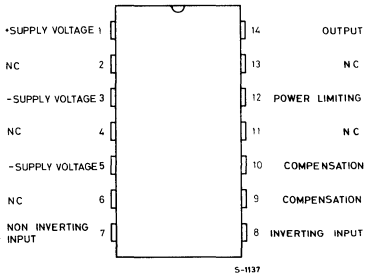
ORDERING NUMBERS: TDA 2020D A82 dual in-line plastic package
TDA 2020D A92 quad in-line plastic package
TDA 2020D AC2 dual in-line plastic package with spacer
TDA 2020D AD2 quad in-line plastic package with spacer

MECHANICAL DATA

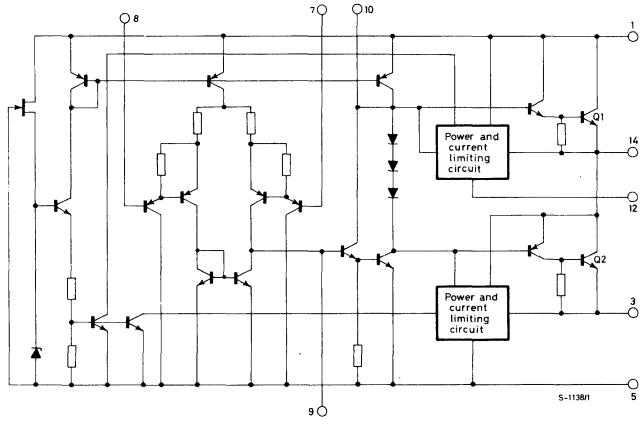
Dimensions in mm



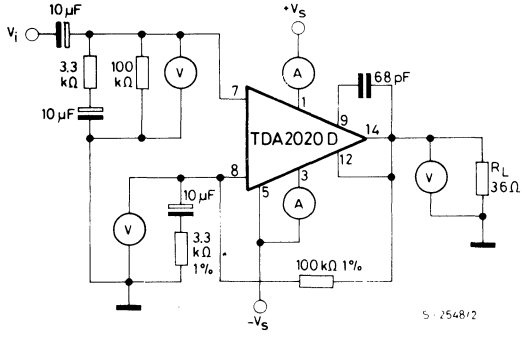
CONNECTION AND SCHEMATIC DIAGRAMS
(top view)



The copper slug is electrically connected to pin 5 (substrate)



TEST CIRCUIT



THERMAL DATA

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max	3	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, V_s= ±20V, T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_s	Supply voltage		± 5		± 25	V
I_d	Quiescent drain current	V_s = ±25V		40	80	mA
I_b	Input bias current			0.15		μA
V_{os}	Input offset voltage			5		mV
I_{os}	Input offset current			0.05		μA
V_{os}	Output offset voltage			10	100	mV
$V_{CE(sat)}$	Output saturation voltage	I_o = 0.5A		± 1.7	± 2	V
B	Frequency response (-3 dB)	I_o = 0.5A		10 to 160 000		Hz
d	Distortion	G_v= 30 dB I_o = 0.5A f = 1 kHz f = 40 to 15 000 Hz		 0.05 0.2	 0.3	 % %
	Intermodulation	DIN 45500		0.2		%
R_i	Input resistance (pin 7)			5		MΩ
G_v	Voltage gain (open loop)	f = 1 kHz		100		dB
G_v	Voltage gain (closed loop)		29.5	30	30.5	dB
e_N	Input noise voltage	B (-3 dB) = 10 to 20 000 Hz		4		μV
i_N	Input noise current			0.1		nA
SVR	Supply voltage rejection	f_{ripple}= 100 Hz G_v= 30 dB	35	50		dB
I_d	Drain current	P_o = 4.5W R_L= 36Ω P_o = 2W R_L= 36Ω		160 100		mA mA
T_{sd}	Thermal shut-down junction temperature			145		°C
T_{sd}	Thermal shut-down case temperature	P_{tot}= 5W		135		°C

Fig. 1 - Quiescent current vs. supply voltage

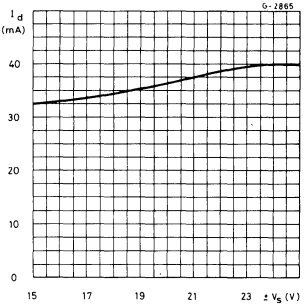


Fig. 2 - Output current vs. $V_{CE(sat)}$

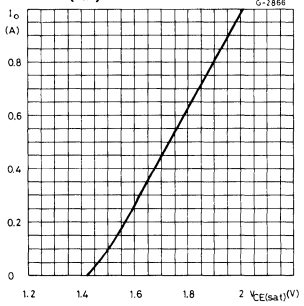


Fig. 3 - Power dissipation vs. supply voltage

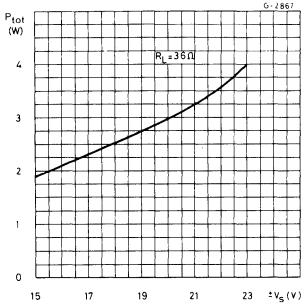


Fig. 4 - Open loop frequency response with different values of the rolloff capacitor

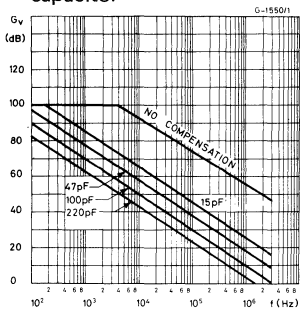


Fig. 5 - Value of rolloff capacitor vs. voltage gain for different bandwidths

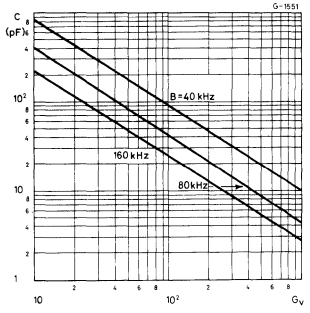


Fig. 6 - Supply voltage rejection vs. voltage gain

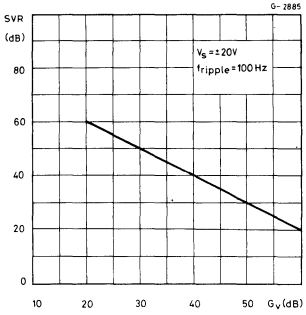


Fig. 7 - Transient response

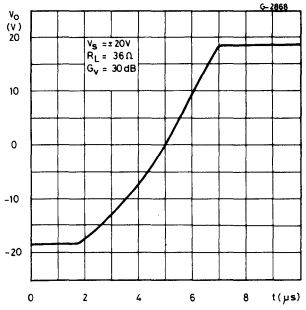
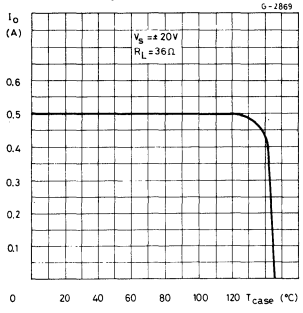
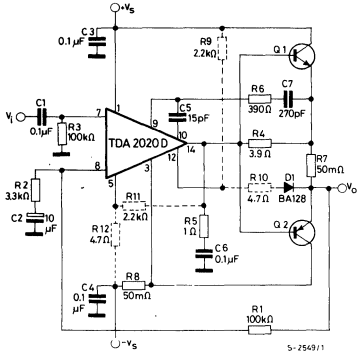


Fig. 8 - Output current vs. case temperature



APPLICATION INFORMATION

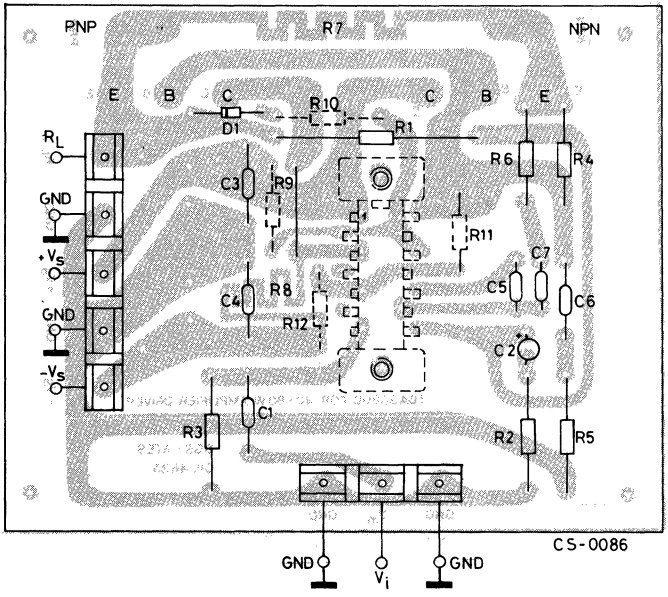
Fig. 9 - Application circuit for P_o= 30 to 50W



Note:
Resistors R9, R10, R11 and R12 are optional. Their purpose is to change the allowable operating area of the output transistors (see fig. 23).
The designer can choose different values according to working conditions (V_s, R_L) and to the SOA of the external transistors. When these resistors are not used the application circuit is modified as follows:

a) R7, R8 are changed to 25 mΩ.
b) R10, R12 are substituted by a short circuit.

Fig. 10 - P.C. board and component layout for the circuit of fig. 9 (1:1 scale)



P_o R_L= 4Ω	30W	40W
± V_s	18V	20V
R9/R11	–	2.2 kΩ
R10/R12	4.7Ω	4.7Ω
Q1	BD707 or BDW21A	BD907 or BDW21A
Q2	BD708 or BDW22A	BD908 or BDW22A

Note:
If resistors R9, R10, R11 and R12 are not used, R7 and R8 must be 25 mΩ. The following table shows what length of wire (copper and constantan) is required to obtain a resistor of 25 mΩ for different values of φ

φ (mm)	1	0.8	0.7	0.5	0.4	0.3
l (mm) copper	–	–	570	290	180	100
l (mm) constantan	40	25	20	10	6.5	–

Application suggestions

The recommended values of the components are those shown in application circuit of fig. 9, although different values can be used. The following table may help the amplifier designers.

Component	Recomm. value	Purpose	Larger than recommended value	Smaller than recommended value
C1	0.1 μF	Elimination of DC current on volume control	Reduced lower cutoff frequency	Increased lower cutoff frequency
C2	10 μF	To obtain DC gain equal to 1	Reduced lower cutoff frequency	Increased lower cutoff frequency
C3 and C4	0.1 μF	Frequency stabilization		Danger of oscillations
C5	15 pF	Upper frequency cutoff	Reduced upper cutoff frequency	Increased upper cutoff frequency
C6	0.1 μF	Frequency stabilization		Danger of oscillation
C7	270 pF	Compensation		Danger of oscillations
R1	100 kΩ	Closed loop gain determination	Larger closed loop gain	Smaller closed loop gain
R2	3.3 kΩ	Closed loop gain determination	Smaller closed loop gain	Larger closed loop gain
R3	R1	Input bias	Output DC offset variation	Output DC offset variation
R4	3.9 Ω	External power transistor driving	Danger of distortion	Increased load for the driver
R5	1 Ω	Frequency stabilization	Danger of oscillations	Danger of oscillations
R6	390 Ω	Compensation		
R7 and R8	50 mΩ	Current protection sensing	Reduced maximum output current value	Increased maximum output current value
R9, R10, R11, R12	see Fig. 23			
Q1 - Q2	BD 707 – BD 708 or BD 907 – BD 908 or BDW 21A – BDW 22A			
D1	BA 128	Short circuit prot.		

Fig. 11 - Output power vs. supply voltage

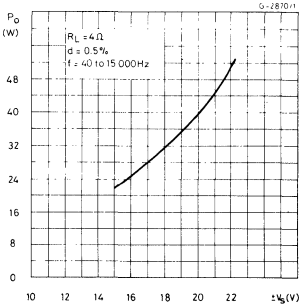


Fig. 12 - Output power vs. supply voltage

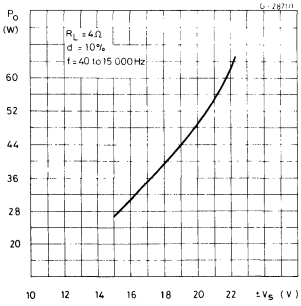


Fig. 13 - Distortion vs. output power

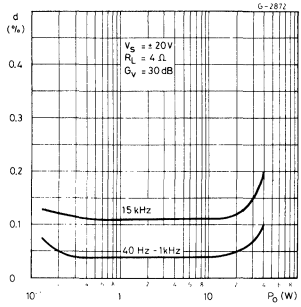


Fig. 14 - Distortion vs. output power

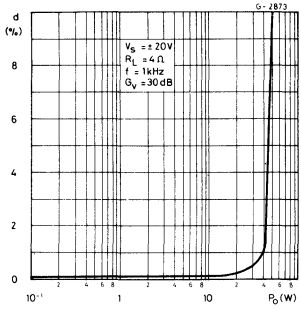


Fig. 15 - Distortion vs. frequency

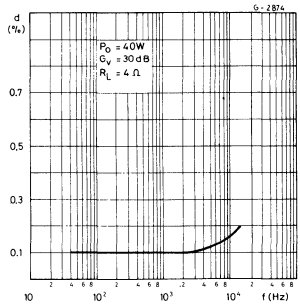


Fig. 16 - Input sensitivity vs. output power

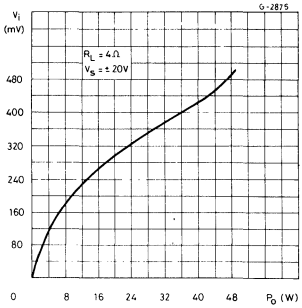


Fig. 17 - Maximum power dissipation vs. supply voltage (sine wave operation)

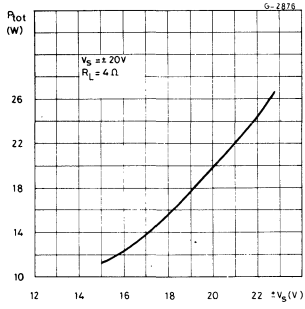


Fig. 18 - Power dissipation and efficiency vs. output power

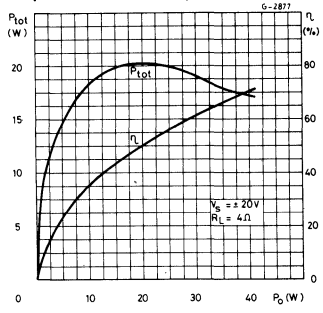
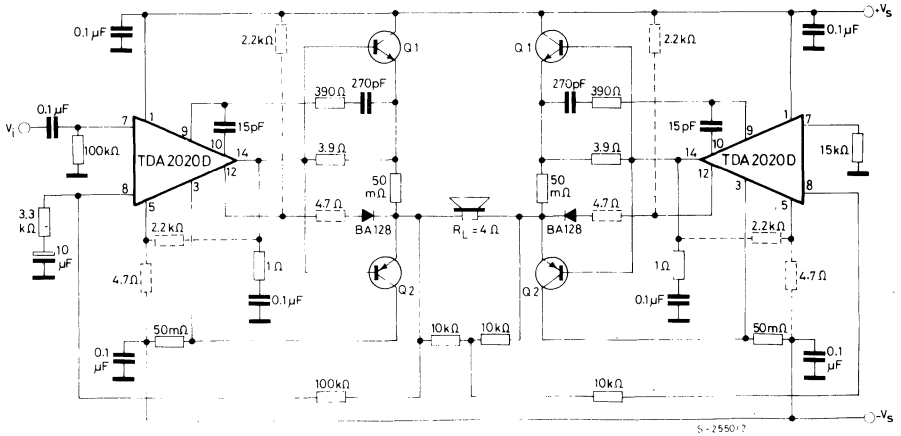


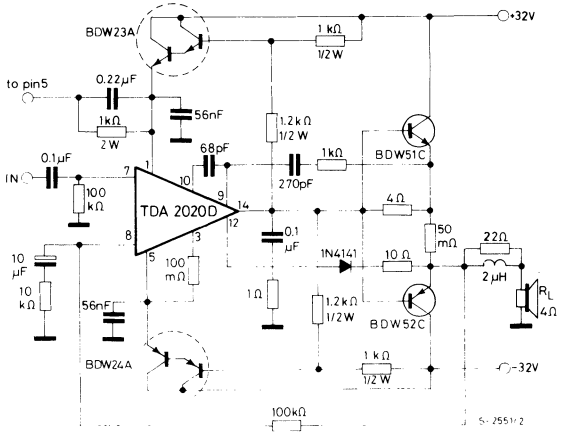
Fig. 19 - 60W to 100W bridge configuration application circuit



Note: With a bridge configuration the output power is increased while the other performances are the same as that of the application in fig. 9. The table shows the output power that can be obtained using different power transistor pairs.

A { Q1 = BDW21A; Q2 = BDW22A; V_s = ±15V; R_L = 4Ω • 60W
B { Q1 = BD707; Q2 = BD708; V_s = ±20V; R_L = 8Ω • 80W
C { Q1 = BDW51A; Q2 = BDW52A; V_s = ±18V; R_L = 4Ω • 100W

Fig. 20 - 80W Hi-Fi amplifier



For this application the maximum value of V_s in no-load condition is ± 45V.

Application suggestions for circuit in fig. 20

Using the two circuits shown in fig. 21 and fig. 22 it is possible to use a transformer with a large spread of output voltage between load and no-load condition.
The voltage on pins 1 and 5 follows V_o according to the equations:

$$V_1 = V_o + (V_s - V_o) \cdot \frac{R2}{R1 + R2} - 2\,V_{BE}$$

$$V_5 = V_o - (V_s + V_o) \cdot \frac{R2}{R1 + R2} + 2\,V_{BE}$$

while the voltage between pins 1 and 5 is a constant. In fact:

$$V_{1\text{-}5} = V_1 - V_5 = V_s \cdot \frac{2\,R2}{R1 + R2} - 4\,V_{BE}$$

$V_{1\text{-}5}$ must not exceed 50V and then the maximum value of V_s in no-load condition will be:

$$V_{s\,max} = (50 + 4\,V_{BE}) \cdot \frac{R1 + R2}{2\,R2}$$

The minimum value of V_s depends on the output power requested and will be:

$$V_{s(min)} = V_L + V_{CE\,(sat)} \text{ with } V_L = \sqrt{2\,P_o\,R_L}$$

Resistance R2 must be greater than R1 to guarantee a positive voltage on pin 1 and a negative voltage on pin 5 for correct working of TDA 2020D.

Note 1 – Between pins 1 and 5 a ceramic capacitor must be inserted to guarantee good stability.

Note 2 – It is possible to insert an electrolytic capacitor (10 μF) between pin 1 and GND and between pin 5 and GND, but in this case the maximum output voltage must be $V_{peak} = 23V$.

With the circuit in fig. 22 the voltage at pins 1 and 5 is kept constant by two zener diodes. In load conditions a current equal to $I_o = I/\beta$ flows in R; the value of R is then given by $R = \frac{(V_{CE} - V_{BE})}{I}\beta$. In no-load condition, if ΔV is the increase in the supply voltage, the zener diodes dissipate a power depending on ΔV and β according to the equation:

$$P_z = V_z \cdot I_z = V_z \cdot \frac{\Delta V}{R} = V_z \cdot \frac{\Delta V \cdot I}{\beta\,(V_{CE} - V_{BE})}$$

Fig. 21

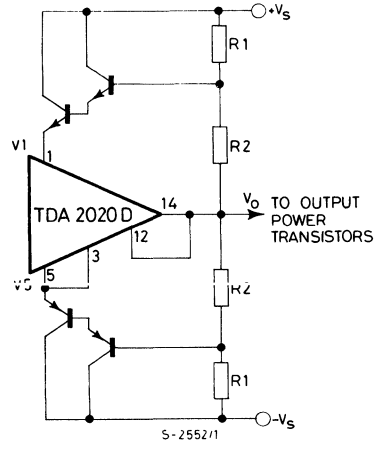
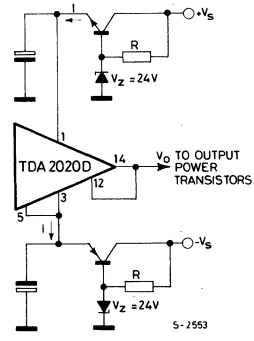


Fig. 22



SHORT CIRCUIT PROTECTION

The most important innovation in the TDA 2020D is an original circuit which limits the current of the output transistors. Fig. 23 shows that the maximum output current is a function of the collector-emitter voltage; hence the output transistors work within their safe operating area (fig. 24). This function can therefore be considered as being peak power limiting rather than simple current limiting.
By choosing the appropriate values for R9, R10, R11, R12, (fig. 9) the maximum output current can be established as a function of the SOA of the output parameters being used.

Fig. 23 - Maximum output current vs. voltage [$V_{Ce(sat)}$] across one output transistor, for different values of R10 (typical application circuit)

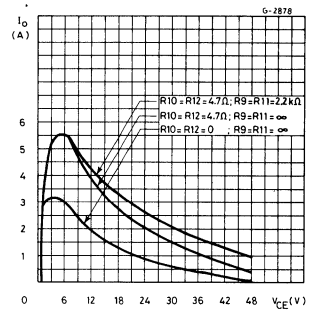
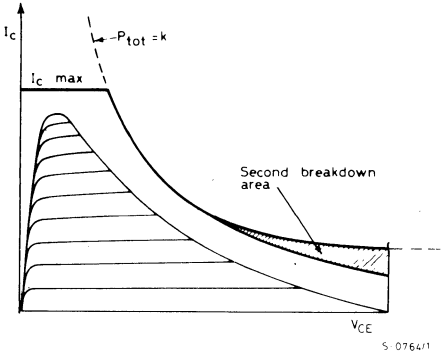


Fig. 24 - Safe operating area and collector characteristics of the protected power transistor



THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent) or an above-limit ambient temperature can be easily withstood since the T_j cannot be higher than 150°C.

2) The heatsink can have a smaller safety factor than a conventional circuit. There is no possibility of device damage due to high junction temperature.

If, for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.
The thermal protection unit of the TDA 2020D will also provide thermal protection of the output transistors if they are mounted on the same heatsink as the I.C.

MOUNTING INSTRUCTIONS

Fig. 25 - Mounting system of TDA 2020D

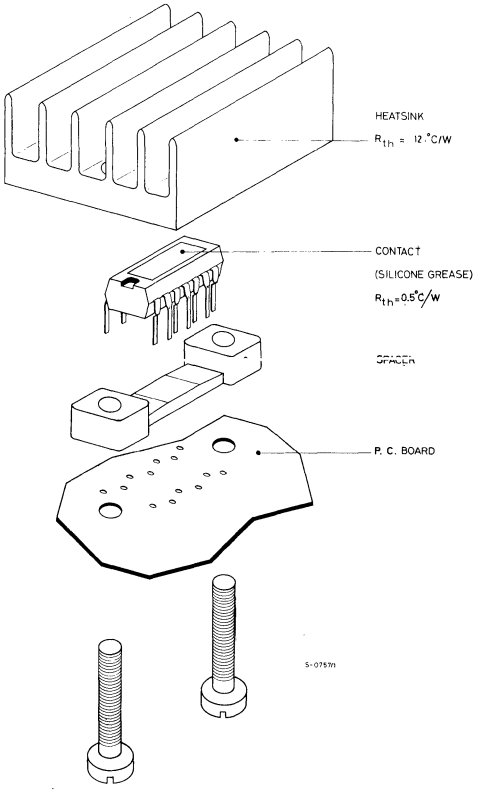
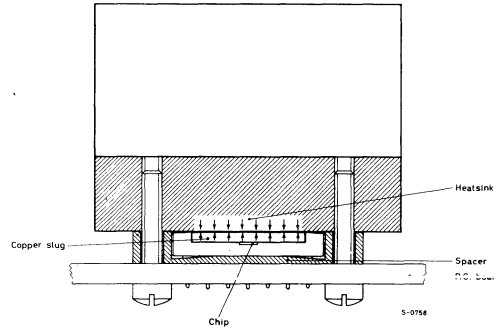


Fig. 26 - Cross-section of mounting system



The power dissipated in the circuit must be removed by adding an external heatsink as shown in figs. 25 and 26.
The system for attaching the heatsink is very simple: it uses a plastic spacer which is supplied with the device.
Thermal contact between the copper slug (of the package) and the heatsink is guaranteed by the pressure which the screws exert via the spacer and the printed circuit board; this is due to the special shape of the spacer.

Note: The most negative supply voltage is connected to the copper slug, hence to the heatsink (because it is in contact with the slug).

Fig. 27 - Maximum allowable power dissipation vs. ambient temperature